A Path Finding Based SI Design Methodology for 3D Integration

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***Abstract*:** 3D integration is being touted as the next semiconductor revolution by industry. 3D integration involves the use of various interconnects that include balls, pillars, bond wires, through silicon vias (TSV) and redistribution layers (RDL) for enabling chip stacking, interposer and printed circuit board (PCB) based technologies. More recently 2.5D integration using silicon interposers has gained momentum as a viable solution for 3D integration. For such new integration schemes to be viable, mixing and matching of technologies is required to evaluate system performance early in the design cycle. The role of path finding is therefore to enable early exploration (planning) prior to costly implementation. Path finding must be based on an efficient electromagnetic analysis (EM) methodology which offers a good balance between speed and accuracy. In this work a hybrid solver is used which combines the Method of Moments (MoM) technique with specialized basis functions and the Partial Element Equivalent Circuit (PEEC) method to accurately provide design guidance.

Three types of test cases are used to explore key implementation areas. The impact of local interconnection density and routing topology for a 2 or 3 layer low cost Silicon interposer technology is investigated. Eleven signal lines are routed within a PWR/GND mesh grid for this example where the line width and spacing is varied to determine the variation in performance. A 49 TSV array is implemented in order to analyze near-end crosstalk (NEXT) between various TSVs in the array. The TSV array is varied to determine the crosstalk impact to determine where signals can be assigned. Wirebonds in a PoP (Package on Package) structure are designed to analyze the effect of design variations on performance. It is predicted that classical PCB designs for consumer electronic devices will continue to shrink as PoP implementations prove more advantageous for speed, area, power and weight related issues. The interconnect length and other parameters of the bond wires is varied to determine the impact on SI performance metrics. Various configurations of the wirebond structure have been demonstrated.

While several variations for each of the test cases described above is analyzed to determine the impact on signal integrity and performance, a larger parameter set can be explored using a Design of Experiments (DoE) methodology, which is not covered in this paper. From these findings, a set of rules can be created for detailed implementation. The examples covered show the attractiveness of using an exploratory tool early in the design cycle.

Keywords — path finder, insertion loss, cross talk, TSV, package on package, bond wire

I. Introduction

As the semiconductor and packaging industry moves towards 3D integration, the impact of vertical interconnections is becoming very important. This coupled with high density redistribution lines (RDL) in the layers of the interposer is allowing for high integration density. Three embodiments of vertical integration is shown in Figure 1 namely, a) chip stacking using wirebonds, b) package on package and c) chip integration using through silicon vias (TSV) and interposers. With technologies rapidly changing, modifications of the three embodiments shown in Figure 1 are necessary to meet both the cost and performance targets. Hence, systems of the future will contain a mixture of these technologies, where as an example, ICs can be assembled on to a substrate using a combination of wire bonds and micro bumps with high density redistribution layers on a silicon interposer containing through silicon vias providing the necessary conduit for communication, with a host of other materials and structures providing for an inhomogeneous interconnection environment.

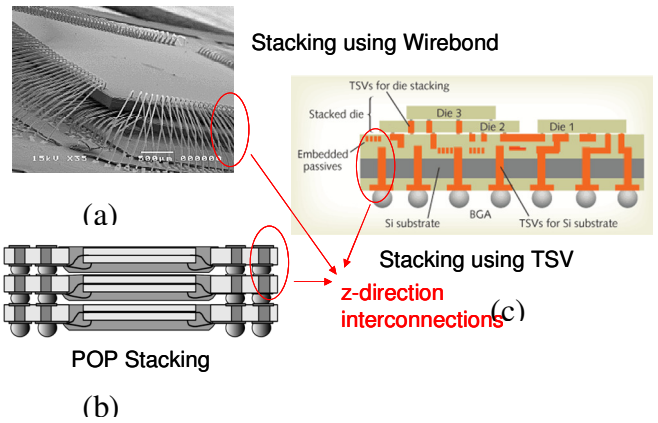

Figure 1: (a) Stacking of ICs using wirebond, (b) Package on Package stacking and (c) 3D ICs on silicon interposer with TSV [1]

Integration of such disparate technologies for a system architect or designer can be challenging since doubts often exist as to whether the combination of such technologies can meet the performance and cost targets required. These doubts can continue even after a combination of technologies is chosen since the structures used in the design needs careful evaluation as to whether they meet the performance targets. In addition process variations and other electrical interactions can make the technologies difficult to implement. The role of path finding is therefore to enable early analysis prior to implementation to minimize expensive modifications to

either the technologies chosen or the structures being implemented. This is illustrated in Figure 2 showing an improved design flow where path finding as an important exploratory tool is shown which can help reduce overall cost of the design cycle.

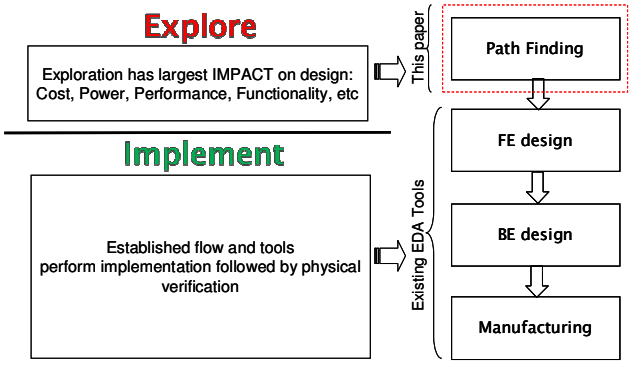

Figure 2: Exploration Vs Implementation and Design Flow [2]

In [2], a path finding methodology for 3D integration was introduced. In this paper details on the model development and hybrid solver is discussed along with examples that elaborate on the application of path finding in the context of vertical interconnections that include wire bonds and TSVs along with redistribution layers in a silicon interposer. This paper is organized as follows: In section II the 3D Path Finding methodology is briefly discussed for completeness along with a description of model development in section III followed by the solver in section IV. Three examples in the context of path finding are discussed in section V with the conclusions summarized in section VI.

II. 3D PATH FINDER (3DPF) METHODOLOGY

A discussion on the 3D path finder methodology is available in [2] which is briefly repeated here for completeness. Consider as an example ICs that are assembled on to a package using wire bonds with the lines routed in the top and the bottom package to create a connection between the ICs. The packages connect to each other through solder bumps. The objective of path finding is to develop a methodology for analyzing the interconnection path by changing the dimensions of the structures (on the fly) so that issues related to signal and power integrity can be assessed early in the design cycle. This may require modifying the diameter of the wire bonds, dimensions of the RDL in the package, diameter of the solder bumps, signal-to-ground ratio, material properties of the package, underfill material between the two packages, to name a few. Hence, the number of alterations to the design is many and therefore a methodology is required whereby a) the structures and test cases can be generated with ease, b) the structures can be analyzed in a reasonable time with manageable memory and c) rules can be developed based on this analysis that can be used for design once the technology options are finalized (not covered in this paper). A lego block concept is used in this paper to create the structures where all the critical parameters are parameterized to generate test cases. Details of model development are described in the next section. It is to be noted that most vertical structures such as wire bonds, vias, TSVs and pillars have cylindrical cross section while the redistribution layer (RDL) has rectangular cross section. In addition, spherical structures such as solder balls can be represented using cylindrical objects. Since the vertical interconnections are critical for 3D integration and are often times difficult to discretize due to the large number of mesh elements required, specialized basis functions are used in a Method of Moments (MOM) formulation to minimize memory and CPU time for analyzing these structures. The RDLs are then meshed using an MOM formulation where the Partial Element Equivalent Circuit (PEEC) approach is used to connect the lateral and vertical interconnection structures together. Details of the solution procedure are discussed in this paper.

III. MODEL DEVELOPMENT

Path Finding requires an evaluation of a large set of alternative solutions to determine which one or ones are suitable for a specific design implementation. This requires any path finding tool to be 1) fast to construct a large set of test cases, 2) support a rigid but flexible methodology; and 3) provide a reasonably fast but accurate analysis.

3DPF, an EDA tool described in this paper, has been developed using the concept of LEGO™ blocks, a toy franchise that has existed for decades allowing kids of any age to imagine and build their creations. LEGO™ blocks allow stacking various sized and shaped blocks requiring minimal instructions or effort. Each block can contain specific via/metal structures and blocks can be stacked to form larger 2.5/3D structures using balls, pillars and/or bond wires. All 3D interconnects are defined as unique profiles and are contained in libraries. The various libraries and profiles can be modified to meet specific manufacturing process electrical and physical requirements. The basic idea behind 3DPF is therefore to allow users to create their own building blocks and then use (and reuse) these blocks to build more complex 2.5/3D structures. Once the various path finding test cases are constructed, each test case's performance can be evaluated against design requirements.

Since 3DPF was specifically developed for 3D integration, three design types are supported namely, Through Silicon Via (TSV), Column Grid Array (CGA) and 3D System. The GUI operations are divided into 3 groups based on frequency of use. The difference between the TSV and CGA based designs is that in the former, the basic building block is a semiconductor while in the latter it is a dielectric, with both supporting through vias. These two design approaches can be connected together in the 3D System using blocks and by adding redistribution layers, wirebonds, solder balls and micro-bumps. Figure 3 shows the methodology used for model development.

In Figure 3, the user first constructs or acquires a library of blocks that can be used to construct 3D systems, where each block has its own electrical and physical properties and can be analyzed separately before its integration into a larger

system. These can be thought of as passive ICs that are constructed with via and metal interconnect layers (without transistors). Blocks can be created in GUI or an ASCII file can be created from various scripting languages such as PERL, TCL, Excel spreadsheets or any Word/Notepad application and imported. In either case, only ports need to be placed prior to analysis. Each block can be used to evaluate the effect of different electrical properties, via profiles/topologies or can be used to connect to other blocks.

To construct the 3D system, all building blocks are imported into the workspace and connected to each other. This could be in the form of stacks (as in 3D integration) or placed side by side (as in 2D or 2.5D integration). The base block is the original 'parent' of the structure. This parent base could be thought as a package, within which all other blocks are arranged using several interconnection schemes.

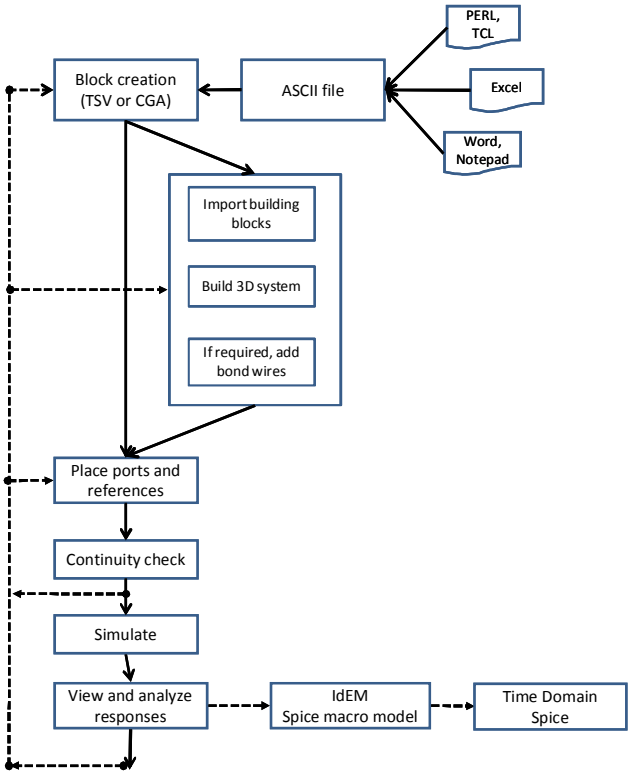

Figure 3: Model Development

Any blocks added become children of this parent. If additional blocks are stacked on these children, they become grandchildren of the base block. Each time a block is added, balls, bumps or pillars can be added at the interface or the interface can be left empty (example is two packages brick-walled to each other). The stack-up design tree can be used to define the parent/child relationship for the individual blocks that form the 3D system. The design tree only affects the Z dimension where the XY dimensions can be suitably aligned with other blocks in the parent/child hierarchy.

As an example consider Figure 4, where the design consists of four unique blocks namely, CGABase, CGA3x3, MemTier and MemCube [2]. Each block contains an array of vias. The blocks are placed on each other with CGABase as the parent and MemCube, MemTier and CGA3x3 as the children. In addition, CGA3x3 is placed as the child to CGA3x3. This parent/child relationship is shown in Figure 4. Also, it is important to note that block CGA3x3 is repeated to create three instances of CGA3x3. Each block before being placed in the system is attached to micro-bumps, and the blocks are then aligned to each other.

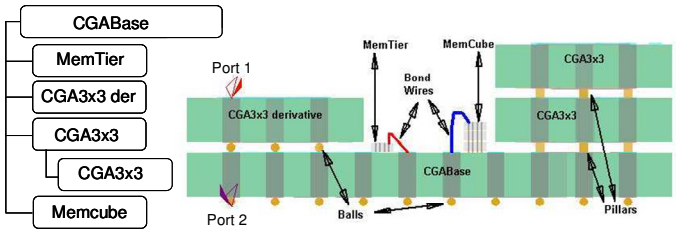

Figure 4: 3D Design showing parent/child relationship

The user can continue to add blocks until all blocks have been added and vertically interconnected. If errors are found during the stacking process, the user can perform *Edit in Place* to correct the errors. When saving individual block edits, the user can either replicate the edits to all blocks with the same name OR create a derivative block (CGA3x3 derivative in Figure 4). If a derivative block is created, only that instance will reflect the changes while all other instances of this block will remain as originally designed. Once all the blocks are correctly placed, bond wires can be added to the design. As with balls and pillars, a library of bond wires can be used for placement which includes custom structures as well.

Two final steps are required before analysis can begin which includes port placement and a continuity check. Ports represent positions where the electrical response can be computed in the form of insertion loss, return loss and cross talk. Continuity checks are similar to DRC (design rule checker), where the physical continuity of the signal path is verified along with the associated references. This provides an elegant method to check for opens or shorts in the design, especially when complicated structures are created.

A design that has passed continuity checks can be simulated to obtain the frequency domain response, which can then be reviewed to ensure if they meet design specifications over the frequency band of interest. Another possibility is to convert the frequency domain response in the form of touchstone files into spice netlists through Idem [3]. Spice netlists can then be used for time domain analysis as well in standard circuit simulators.

IV. SOLVER

After the 3D structure is subdivided into several blocks as described in the previous section, each block can be modeled as a multi-port network by using numerical procedures based on the mixed-potential integral equation. This section summarizes the numerical method, which is composed of three separate procedures, namely 1) modeling dielectric based structures with through vias; 2) modeling of semiconductor based structures with through vias and 3) connectivity between structures to obtain the overall electrical response, which have been deployed in the 3D Path Finder.

Further details on the numerical solution techniques can be found in [1]. Since the most important interconnections in 3D integration are the z-directed wires, special attention is given to the vias during model extraction.

A. *Modeling of Package Interconnections and other Planar Structures in dielectrics and insulators (CGA Block)*

Any block including wirebonds, package vias, column grid arrays (CGA), balls, and planar structures can be modeled by using the mixed-potential integral equation, as in the Partial Element Equivalent Circuit (PEEC) approach. The main difference between the method implemented in 3DPF and conventional PEEC method is that it removes the discretization process for structures with cylindrical cross section by using specialized modal basis functions for capturing current and charge density distributions [5]. Since the required number of modal basis functions is less than seven for wirebonds and vias, the resultant equivalent circuit model becomes simplified, and the modeling of a large number of vertical interconnections in 3DPF [4] becomes possible. As an example, modeling bond wires using the cylindrical modal basis functions are illustrated in Figure 5.

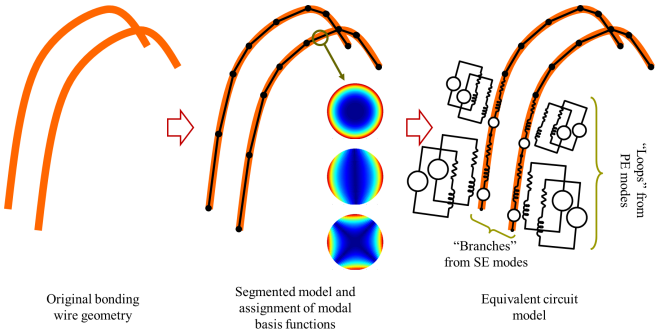

Figure 5: Procedure for modeling bond wires

Planar structures such as microstrip lines, strip lines, pads, and ground planes are modeled using the conventional PEEC method, where the exact interconnection model capturing the thickness effect can be generated. Also, to reduce the computational time, thin-metal approximation that only includes the planar coupling effects can be used (though both the thin and thick metal extraction has been implemented).

The coupling between cylindrical and planar structures requires integration involving piecewise constant basis functions and cylindrical modal basis functions. For considering solid and large ground planes, the image method has been used instead of the PEEC plane model.

B. *Modeling of Semiconductor Substrate with TSVs (TSV Block)*

If part of a 3D structure contains TSV interconnections, it is considered as a separate building block, and the associated TSVs are modeled by using another modeling method, with details available in [5], [6] and [1].

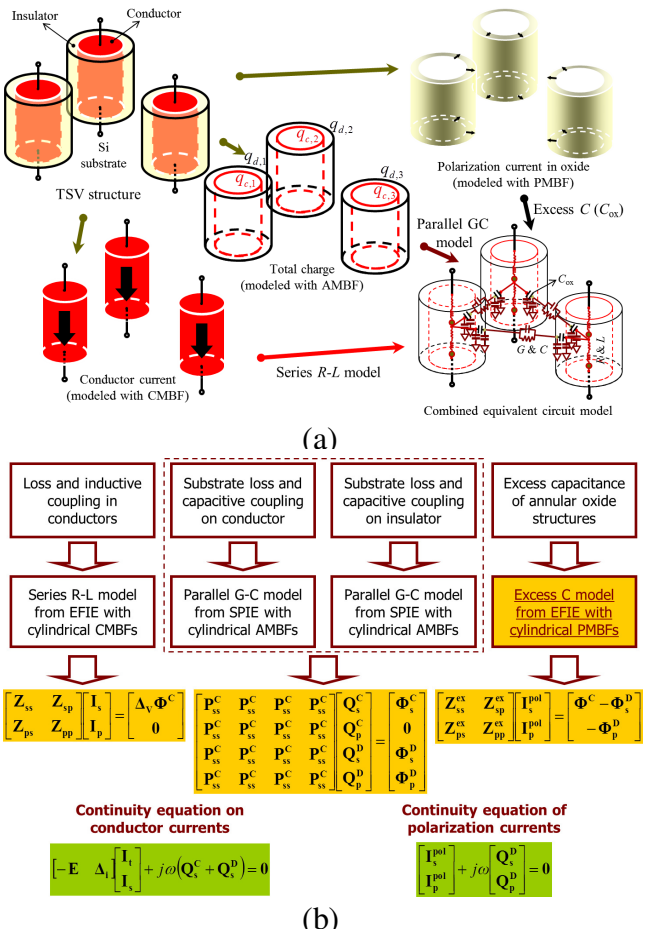

Figure 6: (a) TSV modeling using specialized basis functions and (b) Formulation for modeling TSVs

The TSV modeling method is an extension of the integral-equation-based method in the previous sub-section, where the effects of lossy silicon substrate and oxide liner around each TSV conductor are captured by adding excess capacitors generated with the polarization mode basis functions. The entire TSV model is composed of series resistances/inductances and parallel capacitances/conductances, as described in Figure 6 [1]. Although the generated model is similar to the analytical circuit models based on physics or intuition based methods, the method used in 3DPF is robust and can address the electrical coupling from arbitrary configurations of TSVs. The effect of temperature of the bulk silicon substrate is also considered by including the temperature-dependent conductivity of silicon.

Extension of this method for modeling the depletion effect due to DC biasing is also possible, as discussed in [7]. In addition, tapered vias can be modeled by discretizing the length of the TSVs, which is useful for process optimization.

C. *Node Merging and Port Assignment*

To generate the network parameter model of the entire 3D structure, submodels obtained from the modeling methods (discussed in the previous subsections) for separate blocks should be combined, and ports should be assigned for the overall structure.

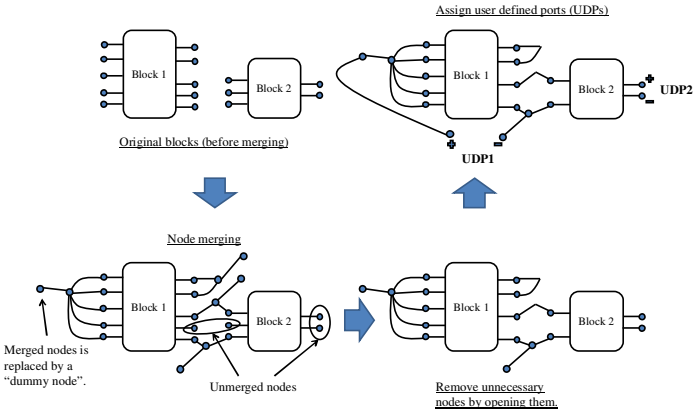

Figure 7: Node merging and port assignment procedure

The process of combining blocks is internally performed through a node merging process, as described in Figure 7. Firstly, some nodes of the original network for individual blocks are merged into a single node. As shown in Figure 7, the nodes to be merged can be in the same block or they can belong to different blocks. After merging, several pairs of reduced nodes are assigned as user defined ports (UDP). The remaining nodes that are not used for UDP are left as open nodes.

V. EXAMPLES

We present three examples in this section using the 3D Path Finder to demonstrate its functionality in the early exploration phase.

Example 1: Comparison of wire bond topologies

In this example, various 1 mil diameter wire bond structures are simulated up to 20GHz to examine impact of: materials (Al vs. Au vs. Cu), wire length (40 mils to 100 mils), wire bond pitch (2.36 mils to 4.72 mils) and impact of return path (location and diameter of PDN wires). The return path is defined as one of the wire bonds contained in Figure 8. As expected, the choice of material had insignificant affect on insertion loss for 40 mil long wires and approached -1dB at 20GHz. All other wire bond simulations were performed using only aluminum (Al) wires.

The insertion loss for the wirebonds is shown in Figure 9a when the length is varied from 40 mils to 100 mils with the frequency response plotted over a frequency band of 20GHz. In Figure 9b, the location of the bond wire and its diameter is varied to understand its impact while in Figure 9c, the effect of wire pitch has been modeled where a tighter pitch results in a lower insertion loss due to the close proximity of the return path. The path finding activity in this example is therefore to understand the impact of various wire bond parameters on its performance.

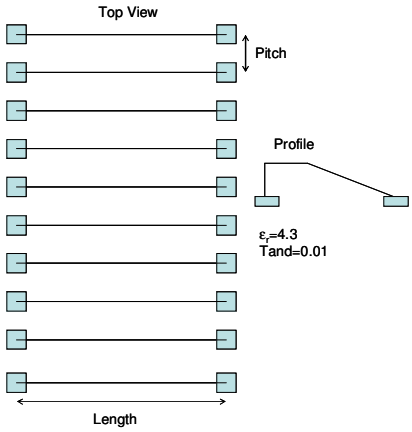

Figure 8: Wirebond parameters

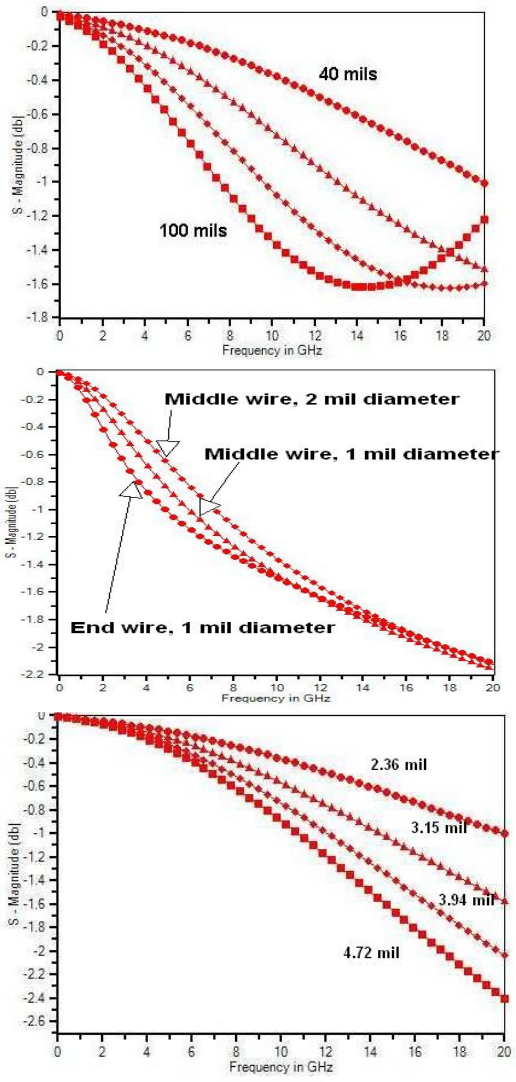

Figure 9: Insertion Loss for Wirebond (a) Top: Function of length, (b) Middle: Function of location/diameter and (c) Bottom: Function of pitch

Example 2: Signal Lines (RDL) and referencing

Consider a group of 11 L-shaped signal lines as shown in Figure 10 with Vss lines beneath it and Vdd lines on the same layer as the signal lines. The bottom layer is a solid

ground plane. The dimensions of the lines and cross sectional dimensions of the structure (3um and 30um thick dielecric) are shown in Figure 10. The dielectric used has a relative permittivity of 4.0. The objective is to compute the insertion loss for the various pitches: 1) Width and space of 3um with unique return paths, 2) Width and spacing of 3um with grouped return paths, 3) Width of 3um and spacing of 7um and 4) Width and spacing of 5um. A more detailed analysis of this structure is provided here as compared to [2].

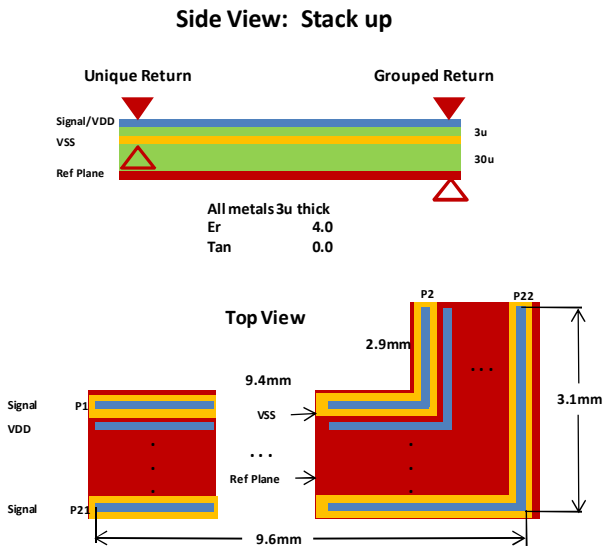

Figure 10: L-Shaped Lines with Vss and Ground reference

The insertion loss for the eleven lines (Cases 1-4) is shown in Figure 11 up to 20GHz. There are several noteworthy effects that can be seen from the figure as follows: For all four cases, each test case has a unique insertion loss profile and significantly degrades in the 4-8GHz range; Unique vs. grouped return paths have dramatic effect on signal line insertion loss due to the return path's lower resistance when grouped; and for this structure, it appears that 3um width and 7um spacing has the best overall insertion loss.

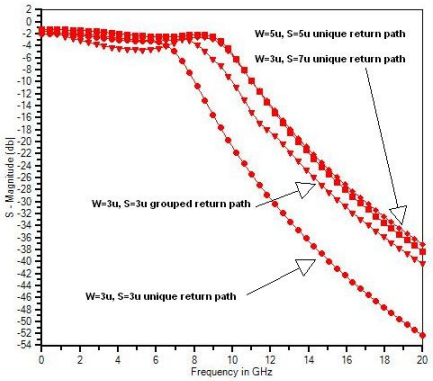

Figure 11: Insertion Loss for the L-Shaped Lines

However insertion loss is only part of the analysis since cross talk needs to be analyzed as well. As shown in Figure 12, Cases 1 and 2 show the effect of grouped return paths on near end cross talk (NEXT). Cases 1, 3 and 4 also show the impact of varying width/spacing combinations. As the separation between signal lines increases NEXT improves as well.

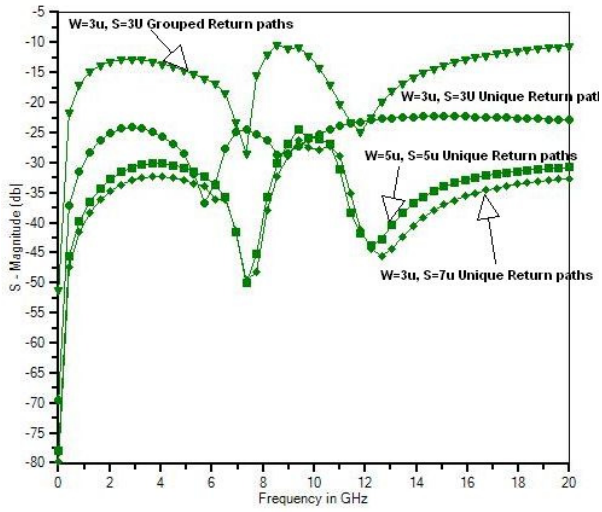

Figure 12: NEXT for L-Shaped Lines

Example 3: TSV Array topology and PDN assignments

This relates to a problem consisting of a TSV array shown in Figure 13a with all physical and electrical parameters provided [2].

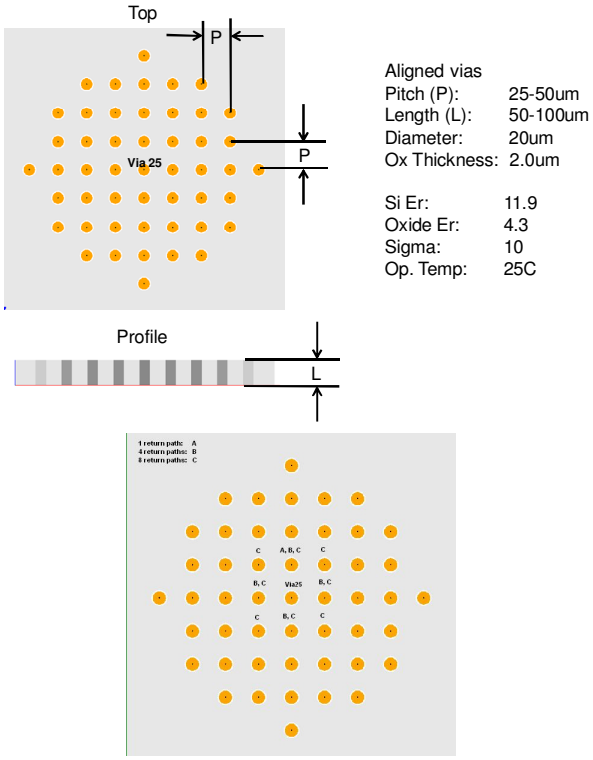

Figure 13: (a) Top: TSV array and parameters and (b) Bottom: Center Via (25) with return path cases A, B and C

The objective is to calculate the coupling between TSVs in the array with uniform cross section with varying via length/pitch and return path configurations (1 vs. 4 vs. 8

return paths). Figure 13b shows Via25 and the three return path test cases A, B and C. Each TSV has ports on top and bottom with infinite references. The first aspect investigated was to determine the effect of length and pitch (maintaining constant via diameter) on cross talk performance. Figure 14a shows insertion loss and Figure 14b shows near end crosstalk (NEXT), respectively.

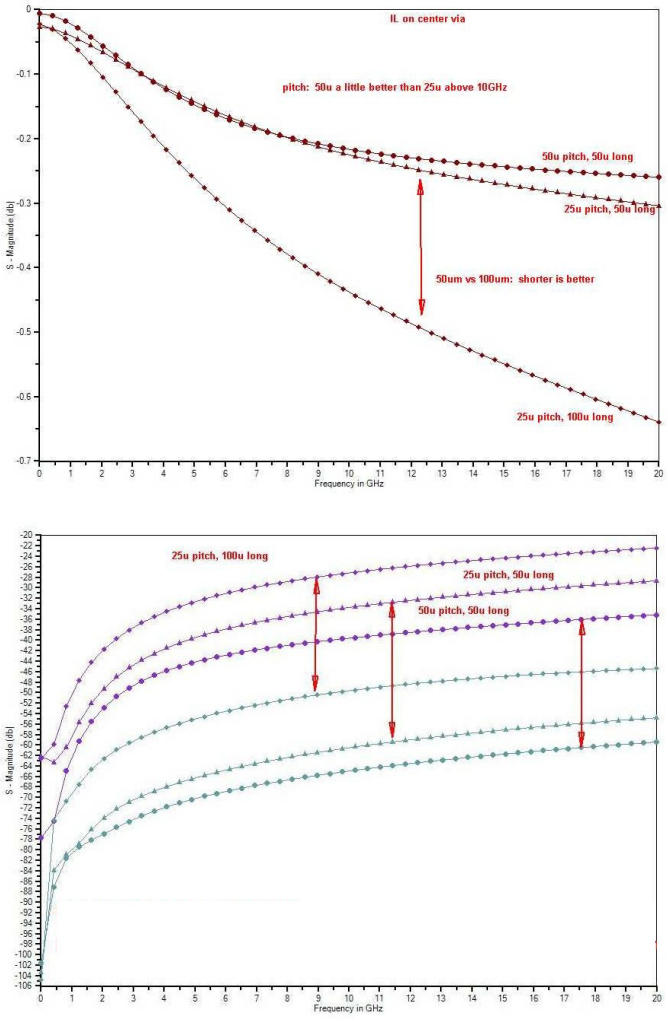

Figure 14: (a) Top: Insertion Loss and (b) Bottom: Near End Cross Talk for 25um Vs 50um pitch and 50um Vs 100um length

In Figure 14a the impact of varying via length with a 25um pitch is shown. Approaching 20GHz, the insertion loss is ~2X worse for a 100um long via as compared to a 50um long via. A thinner silicon wafer will always lead to a better design implementation. In Figure 14b, the worst and best near end cross talk (NEXT) is shown for each configuration. This shows that a wider pitch coupled with a shorter via length reduces NEXT by ~15dB.

Another aspect investigated was the three return path test cases and their impact on NEXT. In Figure 15, the NEXT responses for each test case are shown. The NEXT is measured from the center via to a via next to the return path via. As can be seen, Case A with a single return path has the maximum cross talk on a nearby via whereas Case C with eight return paths has the least. Through path finding analysis, a design's specific signal and PDN assignment can be defined to minimize the performance impact.

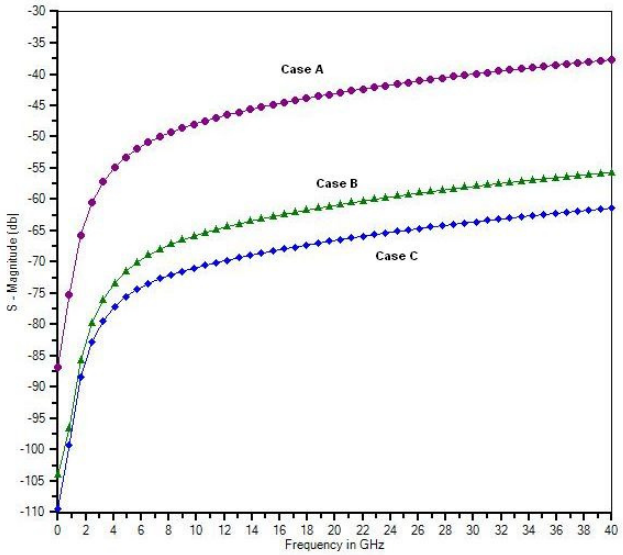

Figure 15: NEXT for different return path cases

VI. CONCLUSION

In this paper, a path finding methodology has been introduced for assessing electrical performance in the context of 3D integration early in the design cycle. The model development is based on a lego block concept where all the critical variables are parameterized for generating test cases easily. This is then used for analysis using an electromagnetic solver specifically developed for 3D path finding. Several 3D structures have been analyzed to demonstrate the value of path finding for exploration prior to design implementation.

VII. REFERENCES

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