ELECTROMAGNETIC MODELING OF THREE DIMENSIONAL INTEGRATED CIRCUITS

MENTOR GRAPHICS

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INTRODUCTION

Three Dimensional Integrated Circuits (3DIC) are generating increased interest as a way to increase speed and density while reducing power and form factor. System level integration in Package (SiP) has joined "System on Chip (SoC)" as one of the primary mechanisms to drive the electronic industry. Quotes such as "Smartphones and Tablets will increasingly owe their prowess to better chip packaging" [Apte11] are now common, and consortia such as the International Technology Roadmap for Semiconductors [ITRS09], SEMI [3DS-IC], Si2 [Open3D], JEDEC [3D-ICs] have all established committees or focus areas on 3DIC. The challenges to develop 3DIC technologies however are formidable, encompassing supply chains, manufacturing, standardization and design technology.

This paper focuses on a fundamental aspect of design technology for 3DICs: Understanding the electromagnetic behavior of 3D structures and how to model them in practice. It examines novel electromagnetic modeling aspects of 3DICs, in particular the use of silicon substrates such as silicon interposer, redistribution layer (RDL) and Through Silicon Via (TSV). It shows how to model electromagnetic properties of silicon substrates, RDL and TSV, how to capture the physical effects in a full 3D solver, and how to incorporate these models into electromagnetic simulation tools. The paper concludes with some examples that illustrate the techniques we have developed.

THREE-DIMENSIONAL INTEGRATION ROADMAP

Devices such as Xilinx' Virtex®-7 200T FPGA and TSMC's Reference Flow 11.0 show the use of stacked silicon integration technology based on silicon interposers with TSV. The use of such techniques will increase dramatically in the near future, posing interesting technical challenges. The ITRS Roadmap for Assembly and Packaging [ITRS09] states that "Modeling of 3D structures", "Through Silicon Vias (TSV)" and "3D tools for System in Package (SiP)" are among the difficult challenges for the decade to come. Multiple 3D techniques are being used, driven by the necessity of higher densities, shorter interconnects and lower power. Examples include mounting ICs on a Silicon interposer, stacked dies and package-on-package (PoP). through silicon vias (TSVs) are used to connect the different levels in several of these technologies:

- Coarse TSV are used for die-to-ball interconnection, such as in Wafer-Level Packaging. Coarse TSV have a pitch of the order of 25-250 µm
- Fine TSV are used for die to die interconnect and have a pitch in the order of 0.5-10 µm

Advanced substrates, silicon interposers and redistribution layers all have feature dimensions in the micrometer range, as small as 10µm and as large as several hundreds of micrometers and they are not expected to shrink by more than perhaps by a factor of two in this decade. These 3D structures are large compared to on-chip dimensions and need to be modeled electromagnetically to take into account inductance and high-frequency effects. In addition, silicon resistivity, loss and capacitance (potentially depletion capacitance in silicon) need to be modeled.

THROUGH SILICON VIA COMPACT MODELING

Modeling silicon as an "interposer" that serves as a substrate to mount several dies as shown in Figure 1 presents some unique electromagnetic challenges. Silicon is a poor dielectric and also a potential semiconductor. The main concern is to model the coupling between vias in the silicon (TSV) and between vias and the metal redistribution layer (RDL) on the die that connects to it.

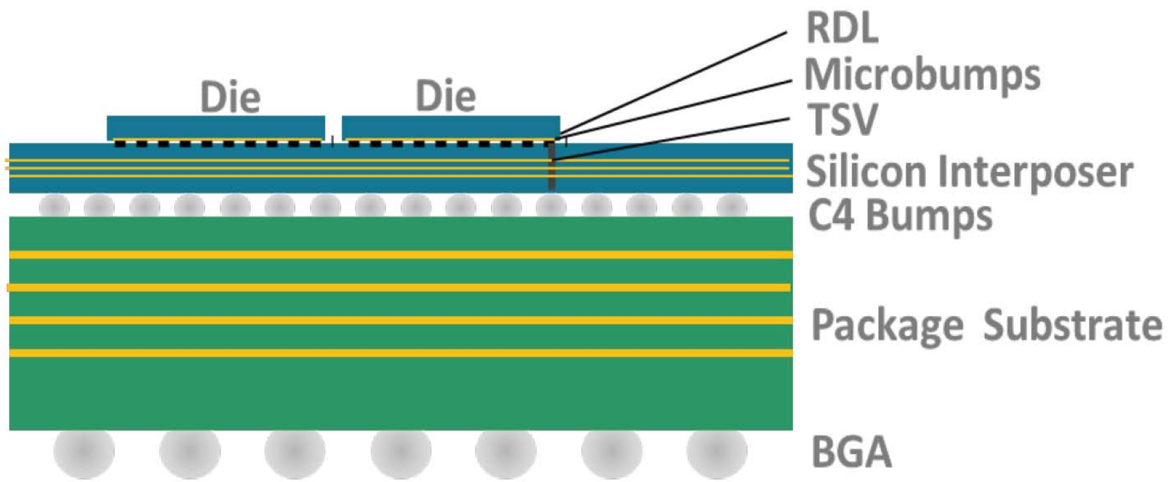

Figure 1. Silicon Interposer with TSV.

The basic idea of analytical models is to generate an equivalent circuit that models the coupling effects and the losses as shown in Figure 2. Note that due to wave effects, in particular due the skin effect, the lumped parameters are frequency dependent.

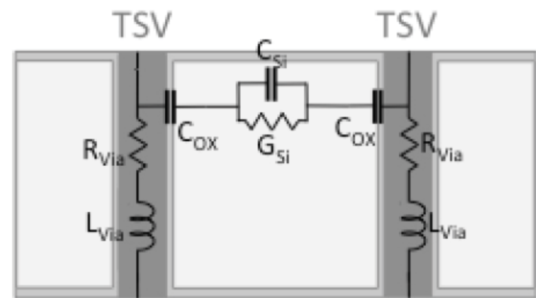

Figure 2: Compact TSV model.

Analytical compact models however have their limitations. In practice, there is little use in modeling just pairs of TSV; the typical silicon interposer will involve modeling arrays of TSV spaced irregularly. In addition TSVs also interact with the RDL, requiring analysis of the coupled RDL-TSV system.

In principle, we can model these structures as three regions: metal (conductor), SiO_2 (dielectric) and silicon (imperfect dielectric with conductivity and permittivity). Additional complexity is introduced by the metal (via) – oxide (TSV liner) – semiconductor (silicon interposer) structure. The metal acts as the electrode of an MOS capacitor. The value of this MOS capacitor can be dependent on the voltage V_{vs} between the via and the silicon interposer and on the frequency of the signal. A complete device-level analysis of the electrical behavior of the MOS capacitor can be found in [Sze07]. In principle, we can distinguish two cases:

- *n-type silicon interposer.* In the typical operating region for $V_{vs} > 0$, the capacitor C_{OX} will operate in accum–ulation. The value of C_{OX} is accurately calculated by modeling the silicon as an imperfect dielectric with per–mittivity and conductivity (as a function of the doping concentration), temperature and electron mobility.
- *p-type silicon interposer.* For $V_{vs} > 0$, the capacitor C_{OX} can operate in depletion or inversion. In depletion, the capacitance is a non-linear function of V_{vs}. However, for all practical purposes, the presence of interface charges Q_{ss} at the Si/SiO_2 interface ensures that in the operating region $0< V_{vs} <1$, the capacitor will work in saturated depletion (inversion) [Katti10]. In inversion, C_{OX} is approximately constant with respect to V_{vs}; however, C_{OX} depends on the frequency. For low frequencies the generation of minority carriers in the depletion region can keep up with the rate of change of V_{vs}, and the capacitance is similar to C_{OX} in accumulation (see above). For higher frequencies (kHz range) the generation of minority carriers cannot keep up with the rate of change of V_{vs} and the depletion region acts as a capacitance in series to C_{OX}, thus lowering the total capacitance. In this case we have to model four regions: Metal, SiO_2, depleted silicon and bulk p-silicon.

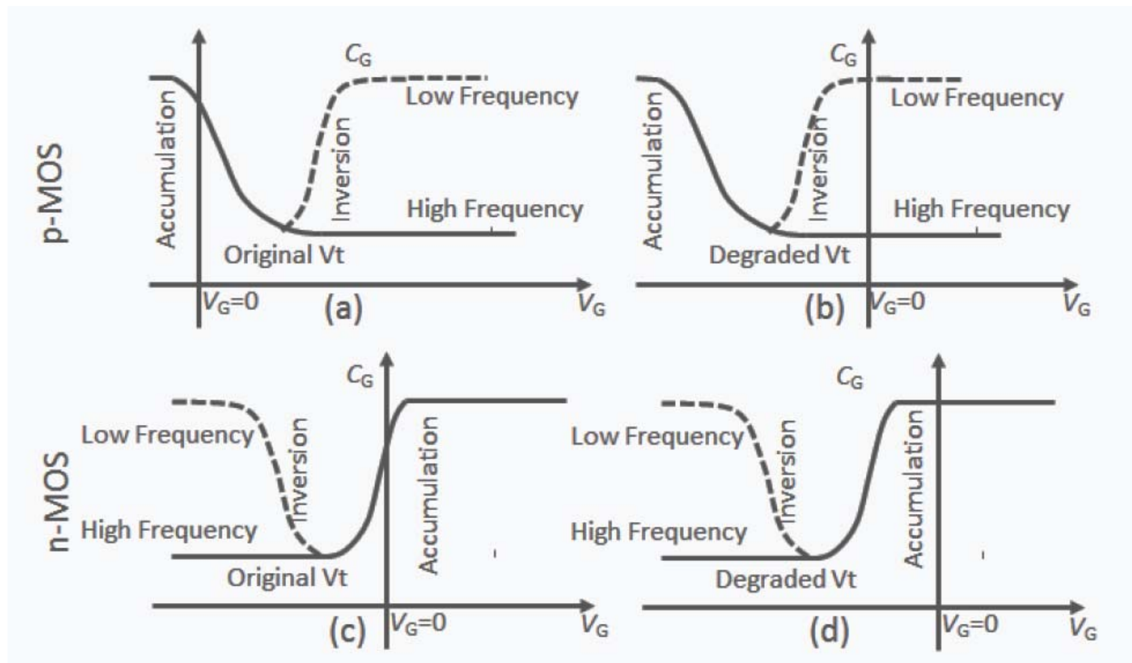

Figure 3. (a) p-MOS original V_t (b) p-MOS with degradation of V_t due to interface charges (c) n-MOS with original V_t (d) n-MOS with degradation of V_t.

TSV ELECTROMAGNETIC ANALYSIS

An accurate electrical modeling of the TSV arrays and merged TSV-RDL structures requires a complete 3D electromagnetic analysis. 3D full-wave simulation engines that accurately capture the frequency-dependant dielectric property of silicon with appropriate conductivity, and model the depletion property for p-substrates to generate broadband S-parameters, can be used for this purpose. However, 3D full-wave solvers simulate many frequency points in discrete or adaptive schemes and can be time consuming.

A 3D quasi-static analysis, in contrast, extracts resistance (R), inductance (L), conductance (G), and capacitance (C), each independently of one another at a given frequency point. 3D quasi-static analysis is therefore much quicker. In some cases, to account for the skin effect, R and L are extracted at DC and at high frequency and an equivalent circuit is synthesized. The C is extracted in an electrostatic formulation with only the real part of the dielectric constant and is therefore assumed constant over the entire frequency spectrum. Hence, in its original form, a quasi-static tool fails to model the accurate broadband characteristics of TSV interactions. The frequency dependence of the dielectric properties of silicon is captured by the following Maxwell equation:

$$\nabla \times H = j\omega D + J \qquad (1)$$

In the case of silicon, which has a relative permittivity (ε_r) of 11.2 and a conductivity (σ) around 10 s/m, the dielectric constant has a significant frequency dependant imaginary component signifying dielectric loss.

$$\nabla \times H = j\omega\varepsilon_0\varepsilon_r E + \sigma E = j\omega\varepsilon_0 E(\varepsilon_r + j\frac{\sigma}{\omega\varepsilon_0}) \qquad (2)$$

To use a 3D quasi-static extraction flow to model,TSV-RDL structures, two main enhancements are necessary:

1. The C extraction needs to be performed with a complex number representation of the dielectric constant. This mode of extraction is often referred to as "C and G together".
2. The CG extraction needs to be performed at DC and high frequency to generate an equivalent circuit with C_{ac}, C_{dc}, G_{ac}, G_{dc} that will appropriately represent the entire spectrum behavior.

It should also be remembered, that the Djordjevic-Sarkar model used for modeling dielectrics with loss-tangent does not apply for dielectrics with conductivity. For an n-type silicon interposer, we obtain values shown qualitatively in Figure 4.

Notice that these results reflect the frequency dependency of R and L due to the skin effect; this effect is not TSV

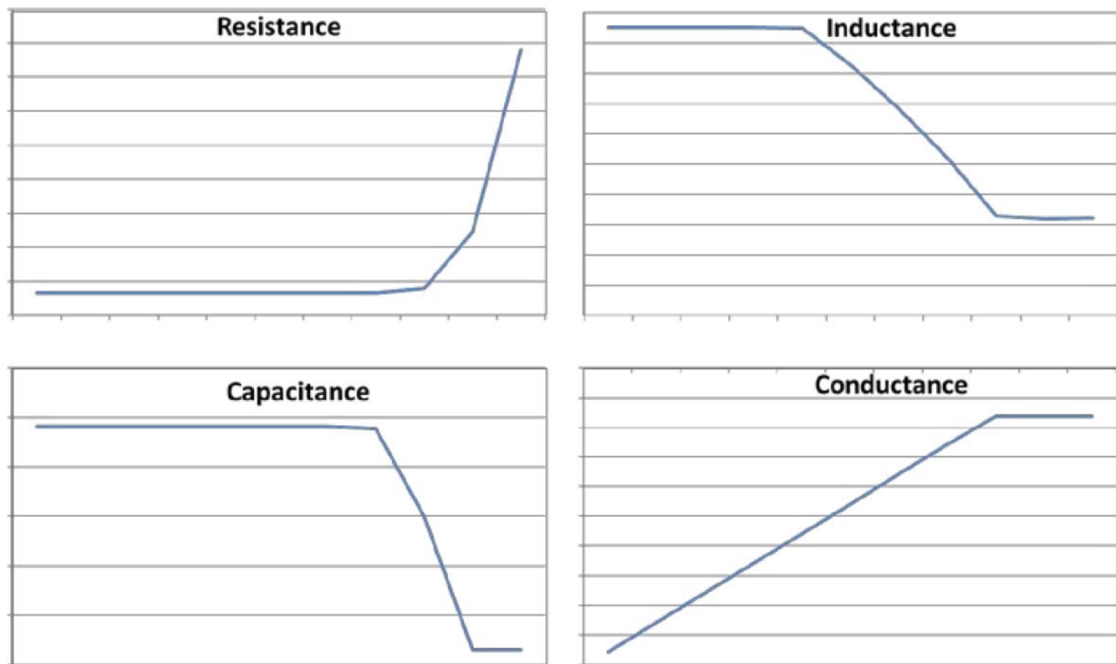

Figure 4. Typical TSV parameters as a function of frequency.

specific and is similar to effects shown in vias or traces in boards and packages that use dielectrics other than silicon as a substrate. The frequency dependence of C and G however is more pronounced and is specific to the use of silicon as a substrate, which behaves more like a dielectric at low frequencies and a conductor at high frequencies. The variation in frequency can be physically explained by analyzing the dielectric component from Figure 2 as shown in Figure 5. The C and G represent the imaginary and the real components respectively of the Y transfer function of Figure 5.

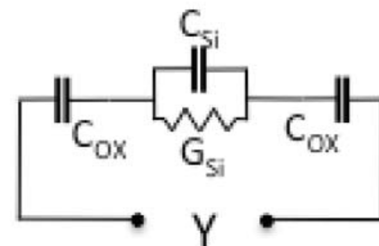

Figure 5. Physical representation of TSV dielectric

EXAMPLES

The following examples are generated using our TSV Bool Creator tool and HyperLynx Fast 3D Solver. They illustrate different effects that can only be captured using electromagnetic solver.

TSV ARRAY 1X11

Using the TSV Bool Creator a 1 x 11 TSV array model was constructed as shown in Figure 6 to study AC inductance and capacitance characteristics at 1 GHz.

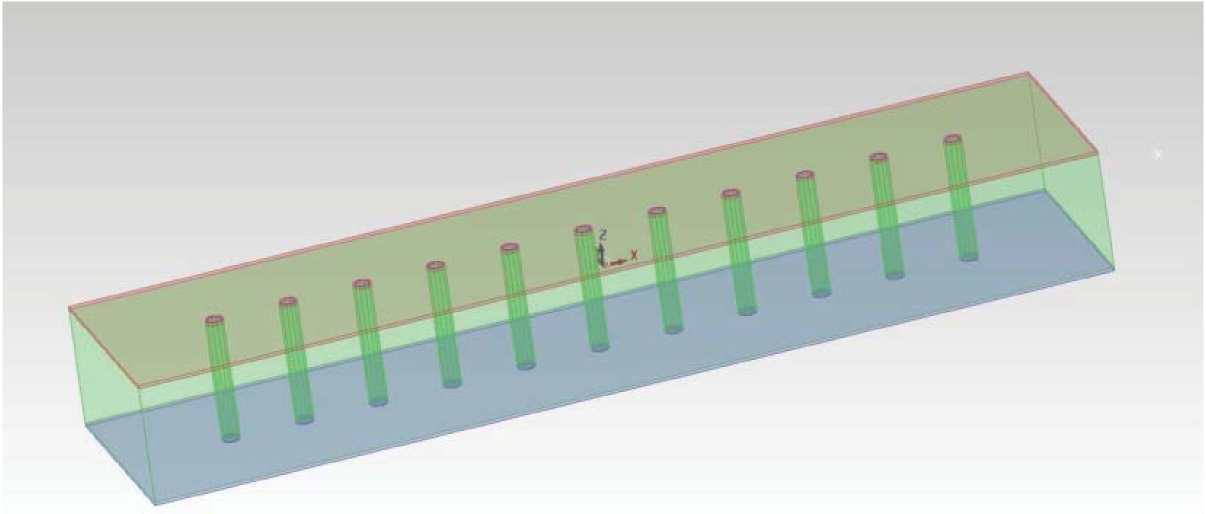

Figure 6. TSV Array 1 x 11.

The full inductance matrix is plotted in Figure 7 while the absolute value of the capacitance matrix is plotted in Figure 8 for improved readability of the negative off-diagonal terms. A few interesting observations:

1. For the inductance array, the self inductance and mutual inductance is similar regardless of whether the via is within the array or on the perimeter of it. The decrease in mutual inductance is consistent on the distance between the vias.
2. For the capacitance array, the self capacitances of the edge TSVs are significantly lower than the vias within the array (one neighbor TSV vs. two neighbors). The capacitances of the vias within the array are consistent.

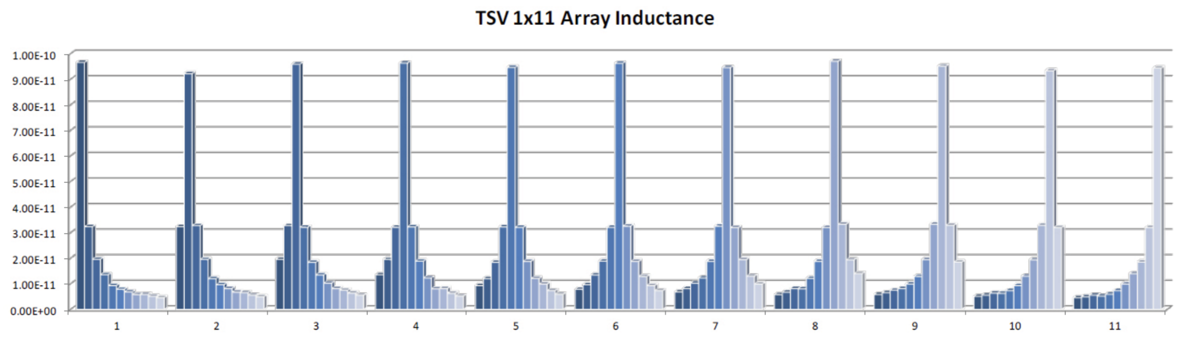

Figure 7. TSV 1 x 11 Array Inductance.

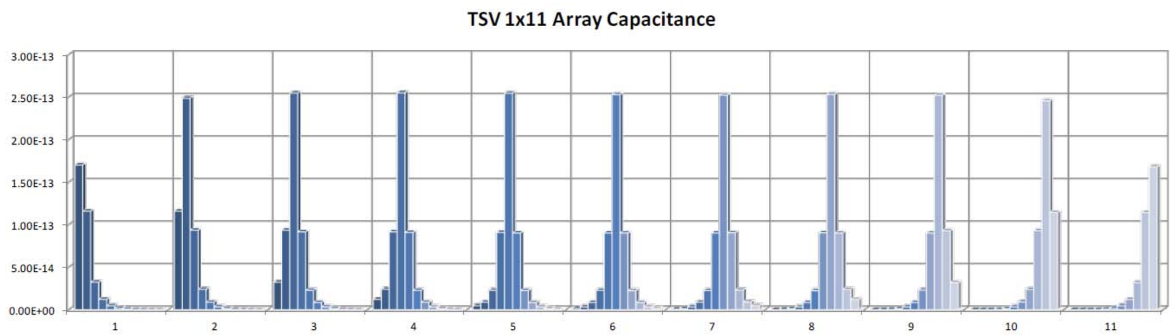

Figure 8. TSV 1 x 11 Array Capacitance.

We can compute the inductive and capacitive coupling coefficients to obtain the normalized inductive coupling coefficients (KL) and capacitive coupling coefficients (KC) values. These are plotted in Figure 9 for non-perimeter TSV. The inductive coupling has larger values and slower decay compared to the capacitance coupling. In Figure 10, we can see how the capacitive coupling saturates its maximum noise within 3 to 4 TSV via distances, however, the inductive coupling has a far greater reach and noise potential.

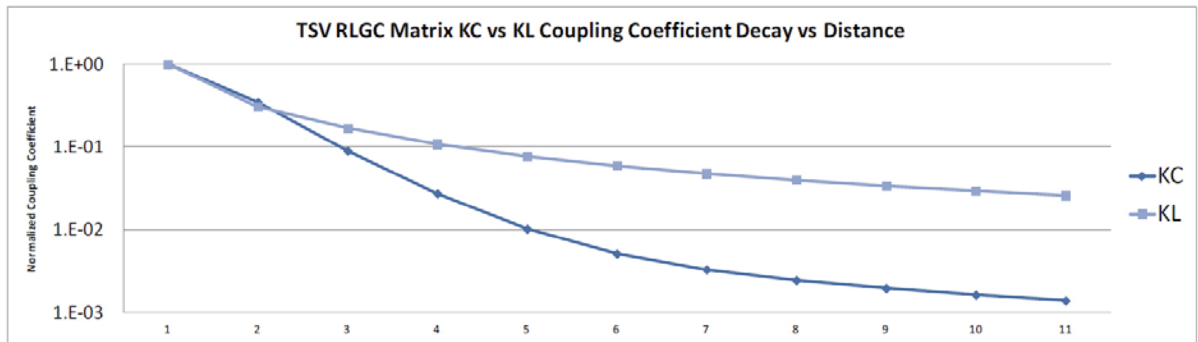

Figure 9. KC and KL Coupling Decay vs. Distance.

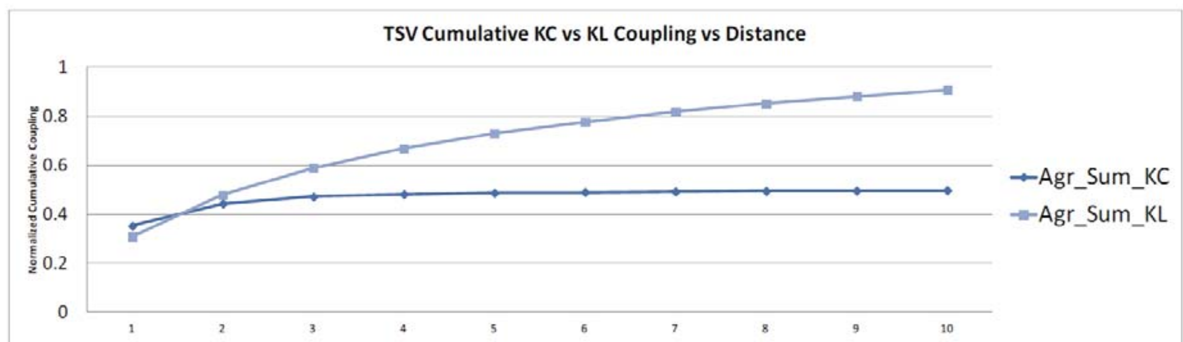

Figure 10. Cumulative KC and KL Coupling vs. Distance.

In Figure 4, we presented the general trend of RLGC as frequency increases, in Figure 11, we can see the self-capacitance matrix values for each of the 11 TSV's as a function of frequency.

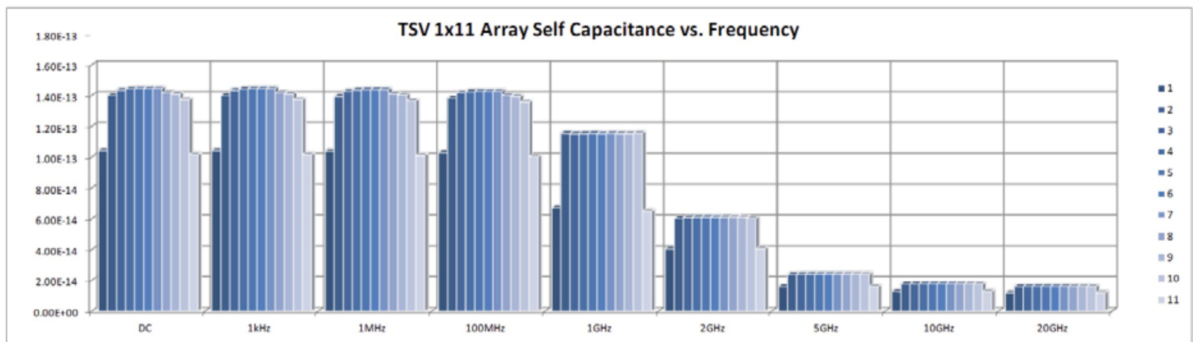

Figure 11. TSV 1x11 Array Self-Capacitance vs. Frequency.

In Figure 12, we have computed and plotted the inductance matrices for three different heights of 160 µm, 80 µm, and 40 µm while adjusting the inductance scale by a corresponding scaling factor. The non-linear scaling of the inductance vs. distance is primarily due to the full 3D nature of the field distribution and it is difficult to capture in general formulas and compact models. When the spatial distribution of these vias become non-uniform, a 3D electromagnetic extractor is essential to obtain accurate performance parameters of TSVs.

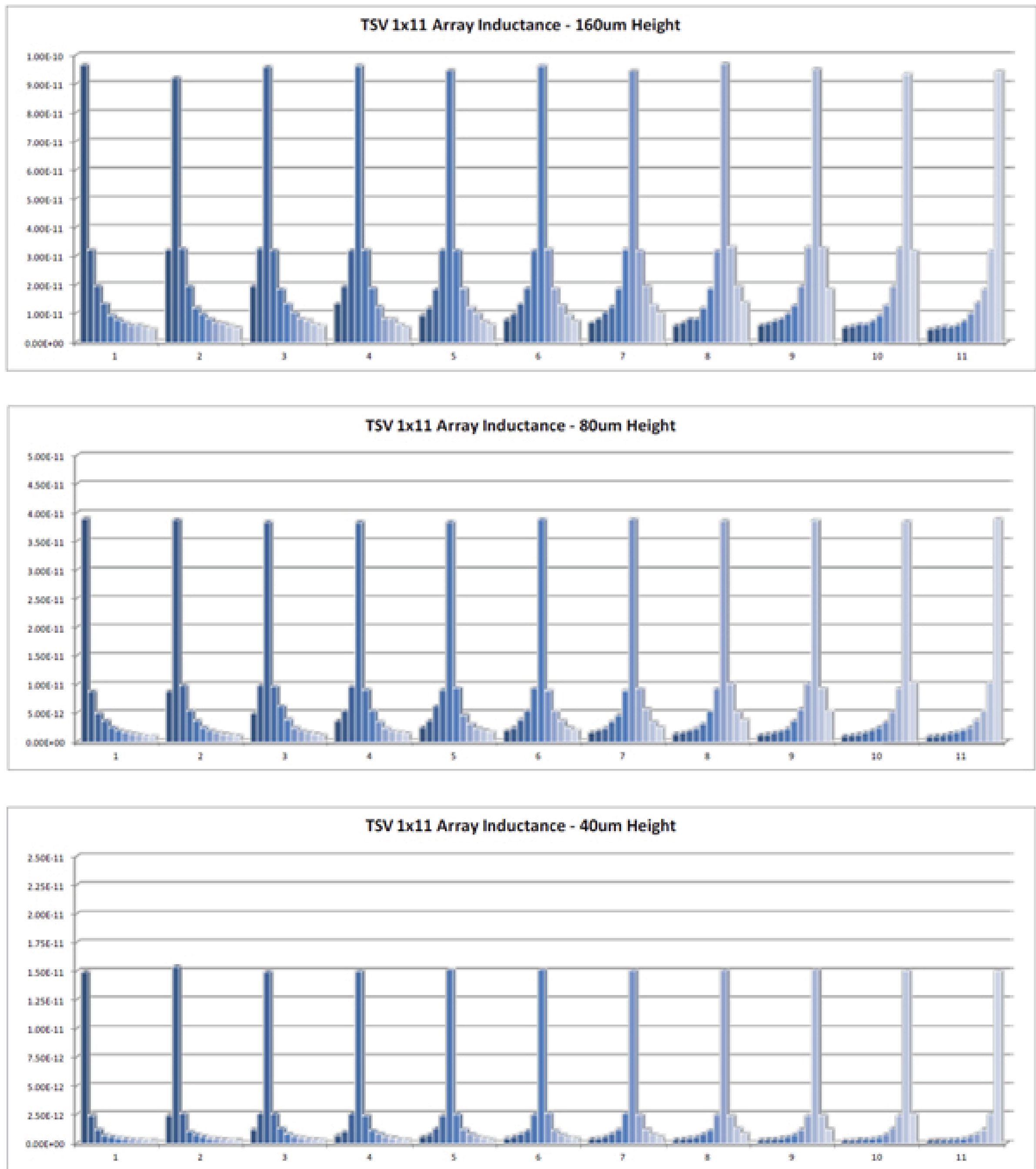

Figure 12. TSV 1 x 11 Array Inductance vs. via height of 160µm (top), 80 µm (middle), and 40 µm (bottom).

SUMMARY

Accurate electromagnetic modeling of 3DIC structures, in particular of dies mounted on a silicon interposer with TSVs, is rapidly gaining importance. These structures differ from traditional packages and boards in that they use finer pitches and silicon as a substrate, requiring the modeling of silicon resistivity, loss and capacitance (potentially depletion capacitance). This paper shows the basic principles to be able to model complex 3DICs accurately utilizing either a 3D full-wave or a quasi-static electromagnetic solver.

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