PACKAGE DESIGNERS NEED ASSEMBLY-LEVEL LVS FOR HDAP VERIFICATION

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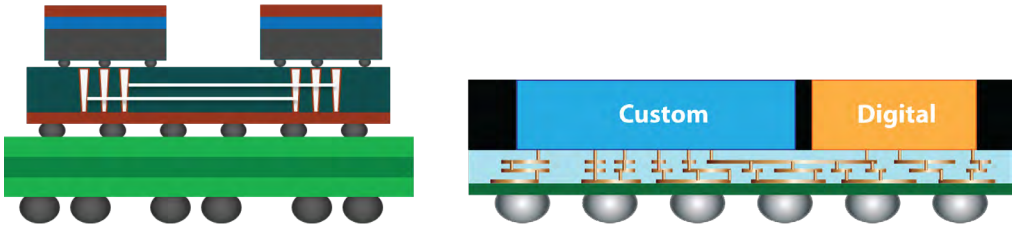
INTRODUCTION

Contrary to what you might think, advanced integrated circuit (IC) packaging is real. Several leading foundries and outsourced assembly and test (OSAT) companies already offer high density advanced packaging (HDAP) services to their customers. The most common approaches currently offered by foundries/OSATs are the 2.5D-IC (interposer-based) style and fan-out wafer-level packaging (FO-WLP) approach (single die or multi die), as shown in Figure 1.



2.5D-IC FO-WLP

Figure 1: The most common package styles currently in use are the 2.5D-IC and the FO-WLP.

Because the interposer in a 2.5D-IC is similar to a traditional die (except that it doesn't include active devices), IC design groups usually owns the 2.5D-IC design, which requires an IC-oriented design approach (Manhattan shapes in the layout database, SPICE/Verilog as the source netlist, etc.). In FO-WLP, IC package groups usually adopt design approaches that are based on spreadsheets (to capture the design intent), in-design manufacturing checks, and (traditionally) no automated layout vs .schematic (LVS) signoff. Automated LVS is not historically popular in the packaging world because the number of components and required I/Os is usually small, so a simple spreadsheet or bonding diagram is sufficient for an eyeball check. However, as HDAP evolves and its use expands, the need for an automated LVS-like flow to detect and highlight package connectivity errors has become apparent.

ASSEMBLY-LEVEL PACKAGE LVS

Although the manufacturing steps and owners for every package technology can be different (2.5D-IC vs. FO-WLP vs. ...), the verification process is almost the same, even if it uses different file formats and tools. An automated package LVS-like flow in its simplest form must ensure that the interposer/package GDSII correctly connects die to die (for multi-die systems) and die to C4/BGA bumps (for both single die and multi-die systems) as intended by the designer. Electronic design automation (EDA) tool suppliers are responding to this growing need with new verification solutions designed to address the specific needs of the HDAP market.

The Calibre® 3DSTACK™ tool provides an integrated verification solution for HDAP inter-die and die-to-package/interposer design rule checking (DRC) and LVS signoff. It offers a significant advantage over traditional SoC LVS flows, because it can automatically evaluate the unique challenges created by HDAP connectivity verification requirements. With the Calibre 3DSTACK tool, users have a single integrated environment for both package assembly-level DRC and LVS, simplifying and speeding up the package verification flow.

Let's look at some of the most common package verification issues, and how designers can use a solution like the Calibre 3DSTACK tool with automated package LVS capabilities to resolve them.

DEBUGGING CONNECTIVITY ERRORS

Even with a package LVS flow in place, it is still a challenge—especially for package designers—to debug package connectivity errors efficiently, particularly if the number of errors returned is huge. However, there are a few simple questions designers can use to help simplify and speed up the debugging process.

1) Do I have pin naming issues in the source netlist vs. the layout?

This is a typical issue in which the designer uses different pin naming conventions in the system source netlist vs. the interposer/package layout (neither includes dummy resistors). For example, Figure 2 shows two connected pins that are named A (die pin) and B (package pin) in the source netlist. Those two pins are represented by two bumps in the layout: BUMP_A (die pin) and BUMP_B (package pin). Although BUMP_A & BUMP_B may be connected correctly in the layout, the package LVS flow will not be able to identify this as a correct connection, and errors will be flagged because the names are different. When this issue occurs, the package LVS flow probably highlights hundreds/thousands of errors.

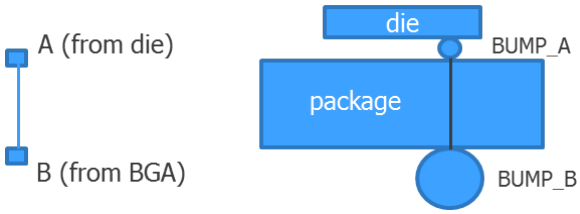


Figure 2: Using different pin names in the source netlist (left)and the layout (right) can make it impossible for the package LVS process to verify the connectivity in the layout.

2) Do I have GDSII export issues?

Database export issues are usually related to packaging-specific flows only (not present in 2.5D-IC). Because FO-WLP manufacturers require a GDSII, rather than traditional package formats (Gerber, ODB++, etc.), most package design tools have now added the capability to export a GDSII of the FO-WLP design. However, this capability is not 100% mature in some package design environments, so it is possible that the exported GDSII includes some faulty data. Common examples include: very small slits in the redistribution layers (RDLs) that are reported as opens in the package LVS flow, or RDL spikes that can connect two different nets (those nets will be reported as shorts).

Typical design rule checking (DRC) checks may not catch those issues, as they are designed to check manufacturability constraints, not GDSII export issues. However, foundries/OSATs should consider delivering additional DRC checks that are built specifically to detect those issues before switching to package LVS flows.

3) Do I have text labels issues?

Before trying to resolve the typical opens/shorts connectivity errors in the interposer/package GDSII, it is highly recommended that the user fixes any “text-related” issues for the pins (usually bumps or pads) first. Examples of these issues (Figure 3) include:

- Layout pins (bumps or pads) with no text label attached to them. Fixing such an error eliminates some “opens” errors automatically.
- Layout pins (bumps or pads) with more than one text label attached to them. Fixing such an error eliminates some “shorts” errors automatically.
- Floating text label that is not attached to any layout pin (bumps or pads).

Layout pins with no text label | Layout pins with multiple text labels | Floating text label

Figure 3: Resolving any text label issues often resolves open/short errors.

Debugging text label issues can be greatly simplified if the package LVS flow reports these types of errors separately.

4) Do I have port mismatch issues?

Extracting a layout netlist from the package/interposer GDSII and performing a source ports to layout ports comparison can identify the following issues:

a) The number of layout ports is larger than the number of source ports. In this case, the extra layout ports are highlighted to the user. As an example, an extra port is reported if layout pins have multiple labels.

b) The number of layout ports is smaller than the number of source ports. In this case, the missing source ports are reported to the user. As an example, a missing port is reported if a layout pin has no label.

Both extra ports and missing ports will be reported if pins are assigned different names in the source netlist and the layout. Again, to minimize debugging time, a package LVS flow should report any port mismatch issues separately from the typical shorts/opens errors.

When these four questions have been asked and resolved, most of the connectivity errors will already be gone. The remaining errors are traditional shorts/opens that require the designer to modify the interposer/package GDSII routing.

POWER/GROUND CONNECTIVITY CHECKING

In traditional LVS flows from the system-on-chip (SoC) world, a design will pass LVS if there is one valid connection for VDD (or VSS), even if there is a broken VDD (or VSS) connection somewhere else. This happens because of the way SoC LVS engines extract the layout netlist. For example, for SPICE format netlists, multiple VDDs/VSSs in the same ".SUBCKT" are reduced to one VDD/VSS. One reason this LVS checking limitation is acceptable in the SoC world is because a broken VDD/VSS connection that is not detected will be caught in future electrical analysis (power analysis, electromigration analysis, etc.). These electrical analysis flows are well established for SoC design and signoff.

For an HDAP with a high number of I/Os, there are typically many die VDD/VSS to package VDD/VSS connections. Using the traditional LVS approach results in the same limitation of being unable to verify all power/ground connections. However, because the electrical analysis flows are not 100% established for HDAP signoff, designers can't neglect those power/ground issues by assuming they will be detected downstream. Fortunately, there are some proposed solutions for this limitation:

HIGHLIGHT "FLOATING" BUMPS/PADS GEOMETRICALLY

This approach can be used for a situation in which there is a VSS/VDD open due to a missing interposer or package bump. Using traditional LVS flows, this issue will not be reported, as there are other valid VSS/VDD connections (assuming the rest of VSS/VDD bumps are correctly connected).

An enhanced package LVS flow relies on a DRC-like approach. It highlights any die bump that doesn't have an interacting interposer/package bump, and vice versa. If there is a missing VSS/VDD die or interposer bump (that causes the open) in the assembly, it is highlighted to the user. In Figure 4, the die bumps are aligned on top of the interposer bumps. However, there is a missing VSS interposer bump (bottom left) that is highlighted as an error.

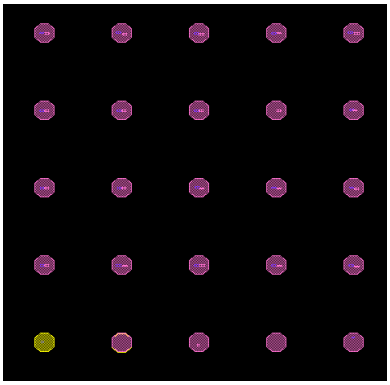


Figure 4: An enhanced LVS flow can find issues like a missing VSS interposer bump.

CHECK LOCATION FOR INTERPOSER/PACKAGE PINS

This technique uses the same geometric checking approach, but also checks that the text labels on the interposer/package bumps are as intended by the user.

Going back to the original source of the problem which is the layout netlisting (reduction of many VSS/VDD pins into one VSS/VDD pin), an enhanced package LVS flow takes advantage of the other netlist formats in the packaging world, like spreadsheets (CSV files) and AIF files. While most package design environments can export such spreadsheets/AIFs automatically, this approach assumes that the enhanced LVS flow also natively supports the spreadsheet netlist format.

In a typical packaging design intent spreadsheet, there are columns representing the pin name, the net name, and the bumps' (x,y) locations (Figure 5). Pin names and (x,y) location information (as intended by the designer) is input to the enhanced LVS flow as the source data. The enhanced package LVS flow compares this source data to the layout to ensure every interposer/package bump is present in its expected (x,y) location in the interposer/package GDSII, and the intended text label (as the pin name) is attached. This way, the enhanced package LVS flow detects any missing interposer/package VDD/VSS pins in the interposer/package GDSII.

Pin Name | Net Name | (x,y) Locations

Functional Signal	Instance Level Name	Design Name	Instance Name	Pin Number	Ref Des	Pin X	Pin Y
AC_MODE	AC_MODE	Package	C4	PAD0	U1	1802.5	1129
BUMP_AC_MODE	AC_MODE	die1	FCCC1	Bump_9_8	A1	776.755	851.61
BUMP_AC_MODE	AC_MODE	die2	FCCC2	Bump_9_8	A2	1676.755	851.61

Figure 5: A package spreadsheet netlist can be used by an enhanced LVS flow to check for missing interposer/package VDD/VSS pins.

CHECK GDSII-ONLY OPENS/SHORTS

This check also evaluates interposer/package pins, but with the assumption that the die bumps are not available for checking. It can be used when designers want to check any VSS/VDD opens in the interposer/package GDSII without including the die pins in the check.

This check uses the text labels in the interposer/package GDSII to check for simple shorts/opens without comparison to a source netlist. If there are two physically connected shapes with

different text labels attached to each, the LVS flow reports a short. If there are two shapes that are not physically connected, but have the same text label attached to them, the package LVS flow reports an open (this check catches any two VSS/VDD shapes that are not physically connected).

HIGHLIGHT BUMPS THAT DON'T HAVE COMPLETE PHYSICAL CONNECTIVITY

Sometimes a VSS/VDD open is not due to a missing interposer/package bump, but is caused by a missing RDL or via polygon in the internal interposer/package connectivity. Traditional LVS flows don't explicitly report such an issue if there are other valid VSS/VDD connections.

To find these issues, an enhanced package LVS flow checks the layout only, without a comparison to the source netlist. If it finds any interposer/package bump (with a text label attached to it as the pin) without complete physical connectivity to the die (using the interposer/package connectivity stack defined in the LVS rules), it highlights this bump as an error.

SUMMARY

With the noticeable growth in high-density advanced packaging (HDAP) technologies, supported by both foundries and OSATs, the desire for an automated LVS-like verification flow for signoff HDAP connectivity verification is now a necessity. Unique package connectivity issues, such as missing or misplaced interposer/package bumps/pads, pin naming and text labeling issues, and the like, require new and enhanced verification techniques that can move across the entire package to ensure proper connectivity and performance.

With its native support for packaging file formats, automated analysis of HDAP connectivity verification requirements, and integrated assembly-level DRC and LVS checking, the Calibre 3DSTACK tool provides a significant advantage over traditional SoC LVS flows. Simplifying and speeding up the package verification flow, while ensuring full coverage and accurate results, supports and encourages the growth of existing and emerging package technologies, and the new and innovative products they can deliver.

For more information,

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