Call for Papers

DATE 2015 Friday Workshop on

3D Integration

Technology, Architecture, Design, Package, Automation, and Test

Grenoble, France
Friday March 13, 2015
http://www.date-conference.com/conference/workshop-w05

General Chairs:
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The **Design, Automation, and Test in Europe** conference and exhibition is the main European event bringing together researchers, vendors and specialists in hardware and software design, test and manufacturing of electronic circuits and systems. **Friday Workshops** are dedicated to emerging research and application topics. At DATE 2015, one of the Friday Workshops is devoted to **3D Integration**. This one-day event consists of a plenary keynote, regular and poster presentations, and a panel session.

WORKSHOP DESCRIPTION

3D Integration is a promising technology for extending Moore's momentum in the next decennium, offering heterogeneous technology integration, higher transistor density, faster interconnects, and potentially lower cost and time-to-market. To produce 3D chips, new capabilities are needed: process technology, architectures, design methods and tools, and manufacturing test solutions. The goal of this Workshop is to bring together researchers, practitioners, and others interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges. Previous editions of this workshop took place in conjunction with DATE 2009, DATE 2010, DATE 2011, DATE 2012, DATE 2013 and DATE 2014.

TOPIC AREAS

You are invited to participate and submit your contributions to the DATE 2015 Friday Workshop on **3D Integration**. The areas of interest include (but are not limited to) the following topics:

- *3D technologies: chip-on-chip, micro-bumping, contactless, and through-silicon-vias interconnect*
- *TSV formation, perm./temp. wafer (de-)bonding*
- *3D architectures and design space exploration*
- *3D combinations of logic, memory, analog, RF*
- *Application, product, or test chip case studies*
- *3D design methods and EDA tools*
- *Signal and power integrity, and ESD in 3D*
- *Thermo(-mechanical) analysis and -aware design*
- *Chip-package co-design for 3D*
- *Test, design-for-test, and debug techniques for 3D*
- *Wafer test access, KGD test, thin-wafer handling*
- *Economic benefit/cost trade-off studies*
- *Standardization initiatives*

SUBMISSION INSTRUCTIONS FOR POSTERS

Submissions are invited in the form of (extended) abstracts not exceeding two pages and must be sent in as PDF file to <weis@eit.uni-kl.de> and <andy.heinig@eas.iis.fraunhofer.de> with "DATE15-3D-WS" as subject. All submissions will be evaluated for selection with respect to their suitability for the workshop, originality, and technical soundness. Selected submissions will be accepted for oral or poster presentation. At the workshop, an Electronic Workshop Digest will be made available to all workshop participants, which will include all material that authors are willing to provide: abstract, paper, slides, poster, etc.

Paper Submission deadline	**November 24, 2014**
Notification of Acceptance	**December 8, 2014**
Camera-Ready Material due date	**February 23, 2015**

MORE INFORMATION

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