Sphinx 3D Pathfinder "Sphinx 3DPF"

Sphinx 3D Path Finder "3DPF" V3.0

Path Finding is a process of exploring alternatives for determining the optimum mix of structures and technologies prior to implementation. "3DPF" is that tool for 2D, 2.5D and 3D integration.

The goal of Sphinx 3D Path Finder ("3DPF") is to explore all the new technologies available for 2, 2.5 and 3D packaging before costly implementation. 3DPF has been specifically developed for path finding thereby allowing expert and non-expert users to easily construct and accurately analyze complex test structures as they hone their implementation guidelines. The real power of 3DPF is to unleash an organization's staff and imagination to fully explore ALL available options while reducing time, cost, risk and resources required.

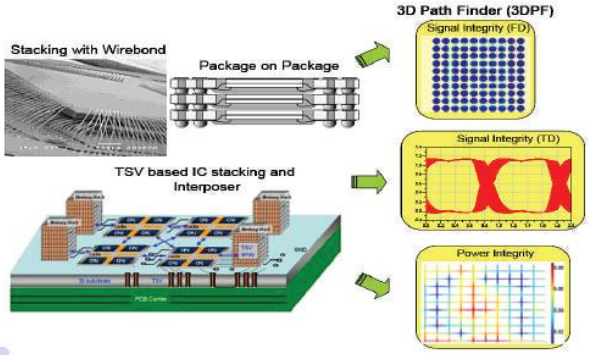

Figure 1: 2.5D and 3D technologies

Supported technologies

3DPF supports various technologies in 2D-2.5D-3D solutions: Through Silicon Vias (TSV), Through Glass Vias (TGV), Redistribution (RDL), Solder bumps (BGA, microbumps), pillars as well as wire bonds. Structures such as: chip stacking, silicon/glass/organic interposers and their interactions can all be constructed and analyzed.

Ultimate freedom to choose

Users can control operating temperatures along with many of the phyical and material parameters when designing structures that meet the electrical requirements. As test structures are analyzed, users can gauge the effect of implementation changes on the overall performance. When path finding is completed, an optimum solution can be chosen long before costly mistakes are found during backend verification.

Growing staff without hiring

3DPF's intuitive GUI provides a LEGO® block based design approach that enables reusability and fast construction of building blocks that are interconnected with balls, pillars or wire bonds, leading to complex 2D, 2.5D or 3D structures. Non-expert to expert users can quickly adopt the analysis methodology and contribute significantly towards decision making.

Does 3DPF have accuracy for the Experts?

Did we forget accuracy? NO. 3DPF's patented algorithm uses method of moments (MoM), specialized basis functions and Partial Element Equivalent Circuit (PEEC) approach thereby accounting for complex parasitic effects due to current flow and charge distribution for both semi-conducting and insulating substrates. 3DPF's accuracy is comparable to full wave electromagnetic (EM) solvers but requires significantly less memory and CPU time as compared to other solvers. Users can EITHER obtain results faster OR can analyze larger structures that otherwise must be 'chopped' to fit into other tools. Either way: 3DPF can be an asset when introduced into a design flow!

Sphinx 3D Pathfinder "Sphinx 3DPF"

Is Process tuning supported in 3DPF?

For users that define manufacturing process specifications, process parameters can be modified to identify 'sweet' spots for maximizing performance and design yields. Along with a robust design, 3DPF allows for the development of a robust process. The parameterized GUI allows for easy analysis of process corners.

What about flows using 3DPF?

The beauty of path finding is that it is at the beginning of the documentation and design flow. Long before logic is designed or transistors are laid out, path finding can help navigate the available technology options. To create flows, 3DPF allows users to create tab delimited ASCII files from scripts, Excel spreadsheets, or Word documents that allow easy support (and documentation) for supporting Design of Experiments (DoE). Both import and export files can be created allowing for Design of Experiment (DoE). In addition, 3DPF creates industry standard Touchstone files that can be converted into macro models for Time Domain analysis. Frequency dependent RLGC parameters for via structures are generated along with continuity checks for complex designs.

What are Users saying about 3DPF?

"Best technical simulation GUI I've every used. It is quick, responsive, logically organized, and intuitive...I do really like it."

- A large Foundry

"Experiments are much easier to set up than with competing tools, dramatically reducing setup time costs."

- A large Semiconductor Company

"Similar to other commercial tool responses, but with less CPU time."

- A large Semiconductor Company

As EUV, FDSOI, FinFET and 450mm wafer solutions continue to struggle with costs and adoption, the industry is migrating towards 2.5D and 3D packaging based solutions. This is the perfect environment and time for using 3DPF!

Learn more about 3DPF and 3D integration from the book "Design and Modeling for 3D ICs and Interposers", M. Swaminathan and K.J. Han; World Scientific Publishing Company, 2013

Sphinx 3D Pathfinder "Sphinx 3DPF"

Case 1:

A small 0.25mm x 0.25mm area in silicon interposer technology can cause considerable coupling in spite of the ground shield used. The ground shield is in the form of grounded TSVs where the RDL layers are affected by the loss of the silicon substrate.

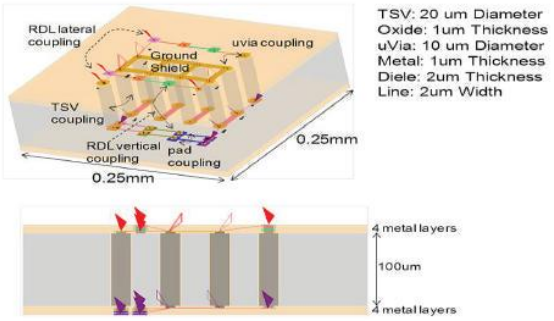

Figure 2: Silicon Interposer in 3DPF GUI

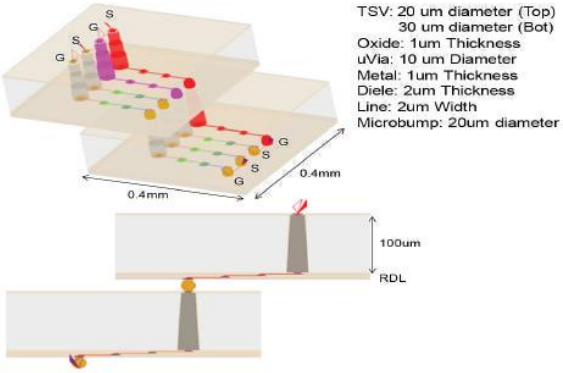

Figure 3: Stacked TSV blocks in 3DPF GUI

Case 2:

TSVs are often tapered due to process conditions with stacking of ICs required to minimize space and enhance throughout. The ICs are connected through microbumps along with RDL layers.

Case 3:

RDL can be used to interconnect ICs on the top metal layer with a ground plane to minimize the effect of the silicon substrate. The TSVs can be used only to supply power and ground to the ICs. Narrow width of the RDL induces resistive losses while the presence of the TSVs can amplify the signal to power coupling in spite of shielding using the ground plane.

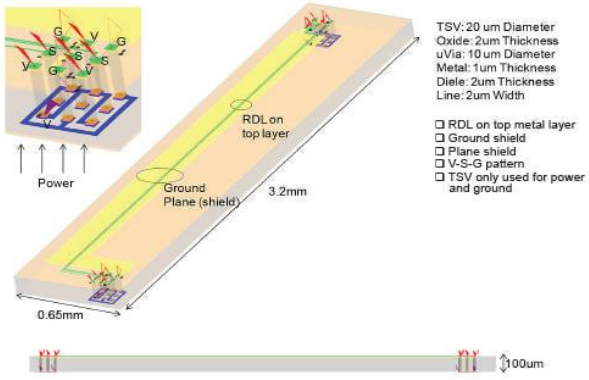

Figure 4: Stacked TSV blocks in 3DPF GUI

For more information on 3DPF visit us at www.e-systemdesign.com.

As the dimensions of the interconnects and thickness of the substrates shrink, two major problems arise - namely, increased losses and coupling. These issues have to be addressed in the context of Signal Integrity, Power Integrity or combined Signal and Power Integrity modeling. With vertical interconnect structures such as Through Silicon Vias, Through Glass Vias and microbumps playing a very important role along with redistribution layers, their effect needs to be addressed as well. Three examples of typical structures that can be analyzed using 3DPF are illustrated above. The results of the analysis are available at: **http://www.e-systemdesign.com/Collateral.html**