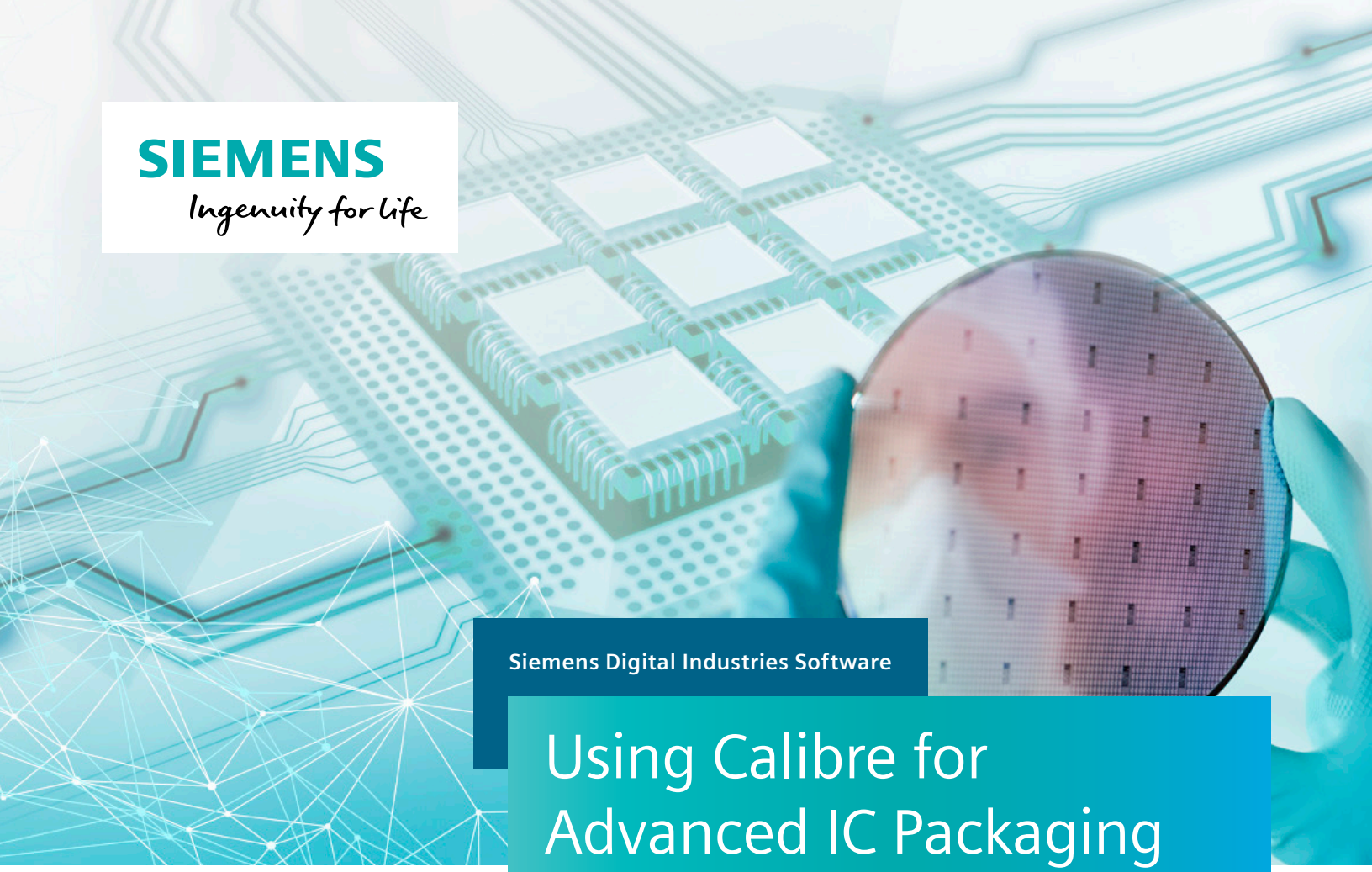

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Using Calibre for Advanced IC Packaging Verification and Signoff

Executive summary

In this paper, we will look at some of the most common package verification issues and how designers can resolve them using the Calibre® 3DSTACK™ tool with automated package LVS capabilities.

Introduction

To satisfy industry demand for continued increases in electronic functions per unit area, foundries and outsourced assembly and test (OSAT) companies have shifted their emphasis to driving packaging innovation. One path is to integrate, in package, smaller, heterogeneous or homogeneous, high-yield chips or chiplets: functional building blocks that when combined provide the same capabilities as a monolithic system on chip (SoC).

Several leading foundries and OSATs already offer such high-density advanced packaging (HDAP) services to their customers. The most common of these advanced technologies are interposer-based 2.5D-ICs and single or multi die fan-out wafer-level packaging (FO-WLP), as shown in Figure 1. These new package types use new materials and processes that are often more similar to silicon wafer fab processes than to traditional organic package substrate processes.

Unfortunately companies adopting these advanced IC packaging technologies often fail to recognize that their legacy approaches to component-level verification do not scale to multi-die, multi-substrate heterogeneous assemblies and, therefore, can result in low yields. Automated layout versus schematic (LVS) checking is not historically popular in the packaging world because the number of components and required I/Os is usually small, so a simple spreadsheet or bonding diagram is sufficient for an eyeball check. However, as HDAP evolves and its use expands, the need for an automated LVS-like flow to detect and highlight package connectivity errors has become apparent.

In this paper, we will look at some of the most common package verification issues and how designers can resolve them using the Calibre® 3DSTACK™ tool with automated package LVS capabilities.

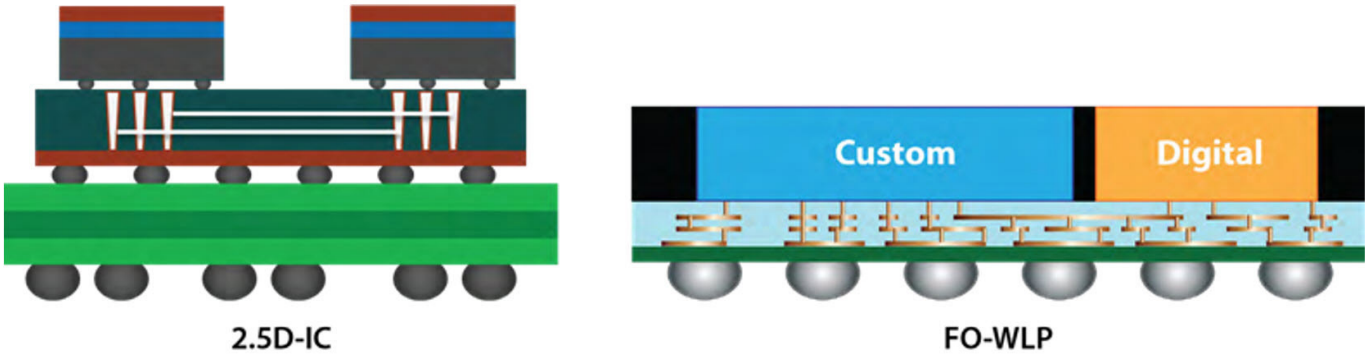

Figure 1: The most common package styles currently in use are 2.5D-IC and FO-WLP.

Assembly-Level Package LVS

Although the manufacturing steps and owners for every package technology can be different, the verification process is almost the same, even if it uses different file formats and tools. In its simplest form, an automated, package LVS-like flow must ensure that the interposer or package GDSII correctly connects die to die (for multi-die systems) and die to C4/BGA bumps (for both single die and multi-die systems), as intended by the designer.

Siemens Digital Industries Software, recognized the growing need for new verification solutions to address the specific needs of the emerging advanced IC packaging market. The Calibre 3DSTACK tool provides an integrated verification solution for HDAP inter-die and die-to-package or interposer design rule checking (DRC) and LVS signoff. It offers a significant advantage over traditional SoC LVS flows because it can automatically evaluate the unique challenges created by HDAP connectivity verification requirements. With the Calibre 3DSTACK tool, users have a single integrated environment for both assembly-level package DRC and LVS, simplifying and speeding up the package verification flow.

Debugging Connectivity Errors

Even with a package LVS flow in place, it is still a challenge—especially for package designers—to debug package connectivity errors efficiently, particularly if the number of errors returned is huge. However, there are a few simple questions designers can use to streamline the debugging process.

1) DO I HAVE PIN NAMING ISSUES IN THE SOURCE NETLIST VERSUS THE LAYOUT?

This is a typical issue in which the designer uses different pin naming conventions in the system source netlist versus the interposer or package layout (neither includes dummy resistors). For example, Figure 2 shows two connected pins that are named A (die pin) and B (package pin) in the source netlist. Those two pins are represented by two bumps in the layout: BUMP_A and BUMP_B. Although BUMP_A and BUMP_B may be connected correctly in the layout, the package LVS flow will not be able to identify this as a correct connection, and errors ill be flagged because the names are different. When this issue occurs, the package LVS flow probably highlights hundreds or thousands of errors.

2) DO I HAVE GDSII EXPORT ISSUES?

Because FO-WLP and other emerging advanced IC packaging processes require GDSII, rather than traditional package formats, most package design tools have now added the capability to export a GDSII for manufacturing. However, this capability is not 100 percent mature in some package design environments, so it is possible that the exported GDSII includes some faulty data.

Two common examples are very small slits in the redistribution layers (RDL) that are reported as “opens” in the package LVS flow, and RDL spikes that can connect two different nets (those nets will be reported as “shorts”).

Typical DRC checks may not catch these issues, as they are designed to check manufacturability constraints, not GDSII export issues. However, foundries and OSATs should consider delivering additional DRC checks that are built specifically to detect those issues before switching to package LVS flows.

3) DO I HAVE TEXT LABEL ISSUES?

Before trying to resolve the typical opens and shorts connectivity errors in the interposer or package GDSII, it is highly recommended that the user first fixes any "textrelated" issues for the pins (usually bumps or pads). Examples of these issues include the following, (shown in Figure 3):

Figure 3: Resolving any text label issues often resolves open and short errors.

- Layout pins with no text label attached to them. Fixing such an error eliminates some opens errors automatically.
- Layout pins with more than one text label attached to them. Fixing such an error eliminates some shorts errors automatically.
- Floating text label that is not attached to any layout pin.

Debugging text label issues can be greatly simplified if the package LVS flow reports these types of errors separately.

4) DO I HAVE PORT MISMATCH ISSUES?

Extracting a layout netlist from the package or interposer GDSII and performing a source-ports to layout-ports comparison can identify the following issues:

■ The number of layout ports is larger than the number of source ports. In this case, the extra layout ports are highlighted. As an example, an extra port is reported if layout pins have multiple labels.

■ The number of layout ports is smaller than the number of source ports. In this case, the missing source ports are reported. As an example, a missing port is reported if a layout pin has no label.

Both extra ports and missing ports will be reported if pins are assigned different names in the source netlist versus the layout. Again, to minimize debugging time, a package LVS flow should report any port mismatch issues separately from the typical shorts and opens errors.

When these four questions have been asked and resolved, most of the connectivity errors will already be gone. The remaining errors are traditional shorts or opens that require the designer to modify the interposer or package GDSII routing.

Power and Ground Connectivity Checking

In traditional LVS flows from the SoC world, a design will pass LVS if there is one valid connection for VDD (or VSS), even if there is a broken VDD (or VSS) connection somewhere else. This happens because of the way SoC LVS engines extract the layout netlist. For example, for SPICE format netlists, multiple VDDs or VSSs in the same ".SUBCKT" are reduced to one VDD or VSS, respectively. One reason this LVS checking limitation is acceptable in the SoC world is because a broken VDD or VSS connection that is not detected will be caught in future electrical analysis (e.g., power analysis, electromigration analysis, etc.). These electrical analysis flows are well established for SoC design and signoff.

For an HDAP with a high number of I/Os, there are typically many die VDD to package VDD and die VSS to package VSS connections. Using the traditional LVS approach on an HDAP results in the same inability to verify all power and ground connections as with an SoC; however, because the electrical analysis flows are not 100 percent established for HDAP signoff, designers cannot neglect those power and ground issues under the assumption that they will be detected downstream. Fortunately, there are some proposed solutions for this limitation.

HIGHLIGHT "FLOATING" BUMPS AND PADS GEOMETRICALLY

This approach can be used for a situation in which there is a VSS or VDD open due to a missing interposer or package bump. Using traditional LVS flows, this issue will not be reported, as there are other valid VSS and VDD connections (assuming the rest of the VSS or VDD bumps are correctly connected).

An enhanced package LVS flow relies on a DRC-like approach. It highlights any die bump that does not have an interacting interposer or package bump, and vice versa. If there is a missing VSS or VDD die or missing interposer bump (that causes the open) in the assembly, it is highlighted. In Figure 4, the die bumps are aligned on top of the interposer bumps; however, there is a missing VSS interposer bump (bottom left) highlighted as an error.

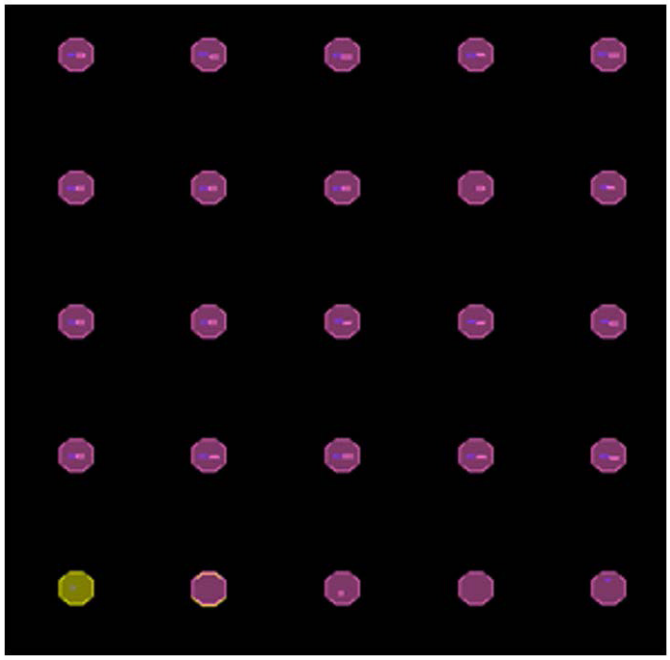

Figure 4: An enhanced LVS flow can find issues like a missing VSS interposer bump.

CHECK LOCATION FOR INTERPOSER AND PACKAGE PINS

This technique uses the same geometric checking approach, but also checks that the text labels on the interposer and package bumps are as intended.

Going back to the original source of the problem, the layout netlisting (reduction of many VSS/VDD pins into one VSS/ VDD pin), Mentor developed the enhanced package LVS flow, which takes advantage of a 3D package, virtual model (known as the digital twin) created using the Xpedition® Substrate Integrator from Siemens Digital Industries Software.

Xpedition Substrate Integrator is a graphical environment for the integration of all the original source data

into a single, golden package assembly model which then drives layout (even if implemented using another vendor's tools) and comprehensive package assembly verification with Calibre 3DSTACK. This digital twin model-driven, enhanced package LVS flow compares the source data to the layout to ensure that every interposer and package bump is present in its expected location in the interposer and package GDSII. It also ensures that the intended text label is attached. In this way, the enhanced package LVS flow detects any missing interposer and package VDD and VSS pins in the interposer and package GDSII.

CHECK GDSII-ONLY OPENS AND SHORTS

The GDSII-only check also evaluates interposer and package pins, but with the assumption that the die bumps are not available for checking. It can be used when designers want to check any VSS and VDD opens in the interposer and package GDSII without including the die pins in the check.

This check uses the text labels in the interposer and package GDSII to check for simple shorts and opens without comparison to a source netlist. If there are two physically connected shapes with different text labels attached to each, the LVS flow reports a short. If there are two shapes that are not physically connected, but have the same text label attached to them, the package LVS flow reports an open.

HIGHLIGHT BUMPS LACKING COMPLETE PHYSICAL CONNECTIVITY

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Summary

With the noticeable growth in HDAP technologies, as supported by both foundries and OSATs, the desire for an automated LVS-like verification flow for HDAP connectivity signoff is now a necessity. Unique package connectivity issues require new and enhanced verification techniques that can be applied across the entire package to ensure proper connectivity and performance.

When combined with the Xpedition Substrate Integrator, Calibre 3DSTACK provides automated analysis of HDAP connectivity verification requirements as well as integrated assembly-level DRC and LVS checking. The Xpedition Substrate Integrator with Calibre 3DSTACK environment provides a significant advantage over traditional SoC LVS flows for HDAP. Simplifying and speeding up the package verification flow, while ensuring full coverage and accurate results, this solution supports and encourages the growth of existing and emerging package technologies, and the new and innovative products they can deliver.

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