Bill Martin
President/VP Engineering
E-System Design

2.5/3.0D packaging: Path Finding

"We're only qualified to 40 degrees ...'what business does anyone even have thinking about 18 degrees, we're in no man's land'" analyses from Bob Ebeling Thiokol[1]

This quote was a ***very costly lesson*** in US NASA's Space Shuttle history. Seven astronauts lost their lives on a decision based on incomplete analysis. The analysis and historical database did not include specific conditions that existed during Challenger's launch on January 28, 1986. Analysis allowed 40 ^{o}F and all previous launch temperatures were above 53 ^{o}F, NO analysis/data existed for below freezing temperatures. Challenger's launch temperature was about 28 ^{o}F.

During the post explosion investigation, we quickly learned about O-Rings: joint seals between solid rocket booster sections. "The causes of the accident fall into two categories: engineering problems ***related to design*** of the joint seal in the solid rocket booster, and flawed decision making procedures related to the launch of the shuttle"[2.]. Product development must look at the overall functionality/performance of a design but also whether the physical structure can support the design's intended function and operating environment. The Challenger explosion was due to a very small physical component in the shuttle program. Much of the Challenger's design was based on proven technologies. US Air Force's Titan III rockets, what had a long, successful history, were used as a model for the Shuttle Solid Rocket Booster. In this case historical successes can breed misplaced complacency. For newer technologies, users must learn how components' affect each other in their specific environment. The next Space Shuttle would not be launched for 32 months as they resolved design, policies and management issues.

How does this translate to high technology products? High Technology continually delivers new levels of product functionality and performance by forcing innovative processes, materials, methodologies and tools into the Design and Supply Chains of providers. The latest smart phones, tablets, eBooks, all coupled with innovative business models and content/app stores are just a few examples. Continually 'pushing' the envelope is what "More than Moore's Law" is about: assembling and composing diverse technologies into a small footprint with minimal weight and power requirements. "More than Moore" is supported by 2.5D or 3D packaging solutions using Package on Package (PoP), System in Package (SiP) and/or TSV/CGA interposers to dramatically shrink or completely eliminate a printed circuit board.

Consumers benefit from this increasing integration. They purchase the latest high tech 'gadget' and are mesmerized by the functionality contained in a small device. Consumers might be aggravated at dropped calls or batteries that need frequent recharging, but show off their latest purchase to anyone. Most consumers are (and should be) oblivious to the complex

technologies integrated into their products to provide these capabilities. This “state of mind” is more than a dream for consumers, it becomes their expectation.

This increased integration causes issues for product developers. Product developers are faced with an infinite set of options and typically use pencil/paper, Excel spreadsheets, or some other – from today’s perspective - arcane method to ‘plan’ their product. A growing number of development teams have migrated to Virtual Prototypes (VPs) to help visualize and analyze functionality and performance of these devices quickly and reliably. VPs help analyze system performance based on hardware/software (HW/SW) trade-offs. But these ***VPs are just a part of the solution and typically do not consider the physical structure*** required to support a product. As with the O-Ring, if small components are incorrectly analyzed, catastrophic issues may come to light during a product’s launch into production. Short lived euphoria can quickly turn into a nightmare for product developers. They face high volume product commitments with little time to debug, fix and re-release the product. Senior management quickly starts calculating the quarterly impact(s) to their P&L, sometimes quantifying the impact on a $s per day basis. ALL involved hope the fix is easy to implement and can be injected late in the manufacturing process. Their worst case fear: re-design of the product from scratch[3].

Are there methods to help analyze a design’s physical structure identifying potential “O-Ring” issues long before implementation? The good news: increasing levels of research are being performed at universities and research consortia concerning “More than Moore” challenges. A new breed of tools is starting to emerge to aid developers in sorting out technical as well as business considerations. They are called Path Finding tools. Think of Path Finding as a Virtual Prototype for a design’s physical structure. Path Finding tools can be applied to three failure mechanisms: mechanical (stress), thermal (heat) and electrical (power distribution, signal integrity) concerns and can include cost estimates as well. Each of these mechanisms must be accounted for in the physical structure of the design. If structural analysis is inadequate, it does not matter what your VP predicted for system functionality and performance, failures occur

To be useful, Path Finding tools must be used EARLY in the planning phase. Using a “post” implementation mentality similar to what is performed for Physical Verification (PV) is too late for these structural issues. Path Finding will never replace PV. Path Finding helps define how something should be implemented most reliable and cost-effective; this does not guarantee that the definition was implemented correctly. For Path Finding to be valuable, it must provide the following:

- Accurate analysis
- Capable of analyzing the entire structure
- Fast creation and analysis of structures
- Capable of supporting many types of structures

Accurate analysis is paramount. If the resulting analysis does not help guide the developer to rules/guidelines that allow a product to yield from manufacturing and normal use, it is a

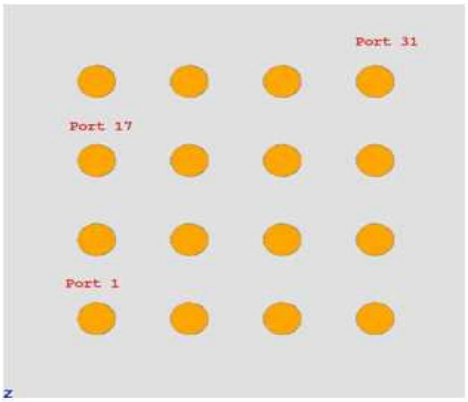
waste of time and money. But accuracy must be based on the specific implementation. The documented research[4,5] states single via simulation cannot be extrapolated for the entire structure's performance (mechanical, thermal or electrical). A short example will be shown in the next section.

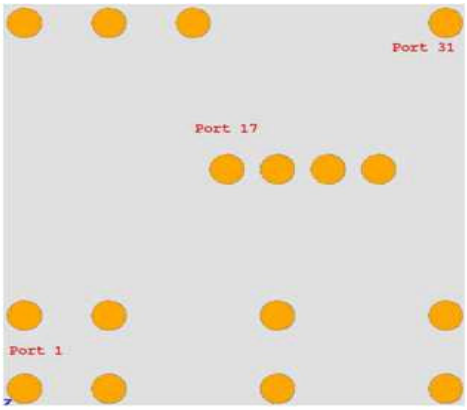
Capable of analyzing large structures is a key to accurate analysis. Without being able to analyze the entire structure, mechanical and thermal interactions or signal integrity analysis will not be accurate. This is directly related how a design is modeled for analysis. Many algorithms use a meshed structure which requires larger memory and CPU time as a design grows in size[6]. Newer algorithms use "meshless" techniques requiring significantly less memory and CPU time enabling entire structures to be analyzed while preserving accuracy. This is especially critical for 2.5/3D packaging structures. If vias are used, developers will maximize via usage within the design to maximize the benefits of: power reduction; performance improvement; area requirements and even overall product costs. As mentioned above, **accurate analysis is not one via at a time but ALL of them and their interactions at one time**.

Fast creation and analysis allows users to quickly identify key manufacturing and/or physical implementation details that meet their specific design's requirements. Each design will have unique physical implementation and signaling that must be analyzed. These constraints might require different implementation scenarios to be analyzed to determine allowable trade-offs.

Support various analyses. Path Finding is about finding viable alternatives. A Path Finder that is relegated to one analysis is less valuable than a Path Finder that can be used in many ways. As an example, process tuning (also called Technology tuning) can be one aspect of Path Finding. A manufacturer may want to perform Path Finding to help optimize their process for mechanical, thermal and electrical, focusing primarily on process parameters they will use in their 'process cook book'. The same Path Finder could be used by a design team to help identify an optimal placement of design structures (i.e. vias) while holding various process parameters constant. A design team that can vary both process and design variables has the ultimate flexibility but requires more analysis. More types of analysis supported allow a wider solution space to be explored for an optimum solution meeting cost, area, performance and power metrics.

Let us look at a short example of a 16 TSV arrayed structure (see Figure 1) related to signal integrity; a vital aspect to a structure's performance. A comparison is performed between a regular (Fig 1a) and a custom (Fig 1b) via pitched design. Besides the via array layout, user also defines other parameters for analysis (Fig 1c). The analysis will be performed on a Full Wave ElectroMagnetic (EM) Solver for accuracy.





Parameter	Value
Operating Temp	25C
Silicon Conductivity	10 S/m
Silicon Permittivity	11.9
Oxide Permittivity	3.9
Oxide Thickness	125nm
Via Conductivity	5.80E+07
Via Length	30um
Via Diameter	5um
Via pitch	25um

(a) (b) (c)

Figure 1: (a) TSV 4x4 array, (b) Custom pitch, (c) parameters used for analysis.

Five variations were created and analyzed with various via dimensions and pitches. Other manufacturing variables could have also been defined for a specific process but were held constant. Figure 2a shows how Insertion Loss varies for each test structure. Insertion Loss (IL) measures the signal's degradation through the via. The smaller the IL, the better the performance will be. In this case the best is the 25um pitch, 15um tall, 2.5um diameter while the worst is 25um pitch, 60um tall and 2.5um diameter. Comparing the five structures against each other for IL, at 4GHz, there is a 3x degradation variation and it continues to widen as the frequency reaches 100GHz. Depending on the application and signaling required, any of these variations might meet the requirements. The variation chosen would both meet the requirements and be lowest in overall costs.

Figure 2b shows the Best and Worst Near End Cross Talk (NEXT) for the structures shown in Figure 1. The NEXT analysis shows how much interference (noise) is transferred between a pair of vias. The location of each via and physical distance from other vias will reflect different NEXT responses for each pair of vias. Vias separated by larger distances will reflect less cross talk between them; closer vias will have larger cross talk. From Figures 2b, variation is widest for the Custom version. Some of the Custom NEXT responses are worse than the standard configuration but a few are better isolated. Whether either will satisfy the goals of this specific design must be determined by the developer. If both could satisfy the requirements the developer can choose the least costly option.

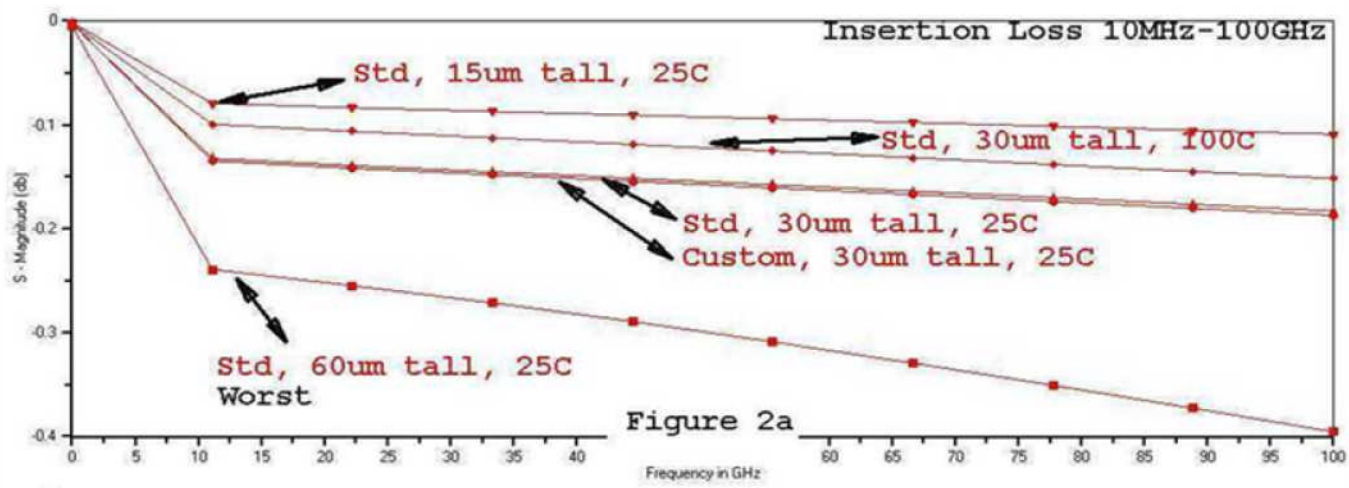


Figure 2a

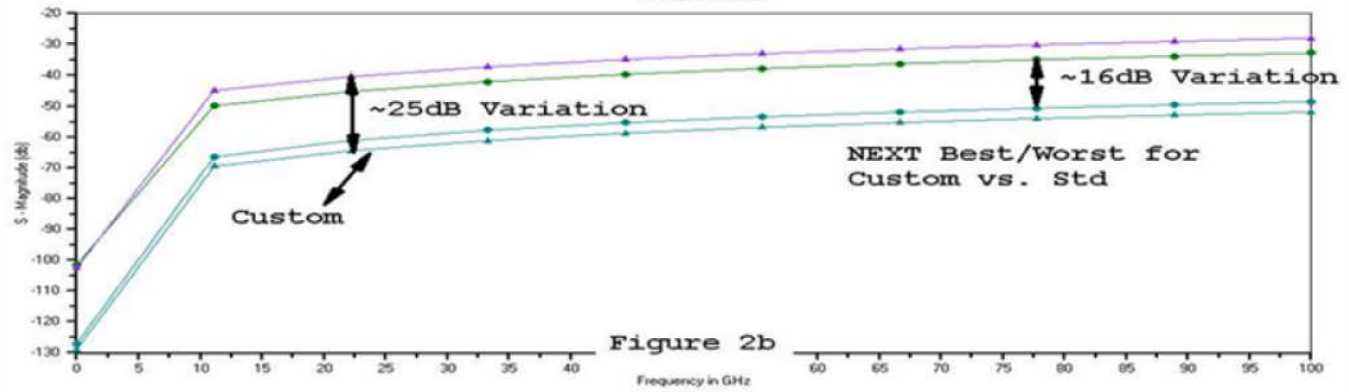


Figure 2b

To view all NEXT responses would total 240, for Far End Cross Talk (FEXT) it would be an additional 240 responses for each structure. To show the NEXT variation for one structure, Figure 3 shows responses for all the TOP vias; this totals 120 responses. This analysis indicates that each unique physical distance between the vias causes a different noise response. For the custom array, this has 25dB variation across all signals. This indicates which via locations might be best suited for noise sensitive signals. In addition this can help define signal to ground ratios as well as shielding needs.

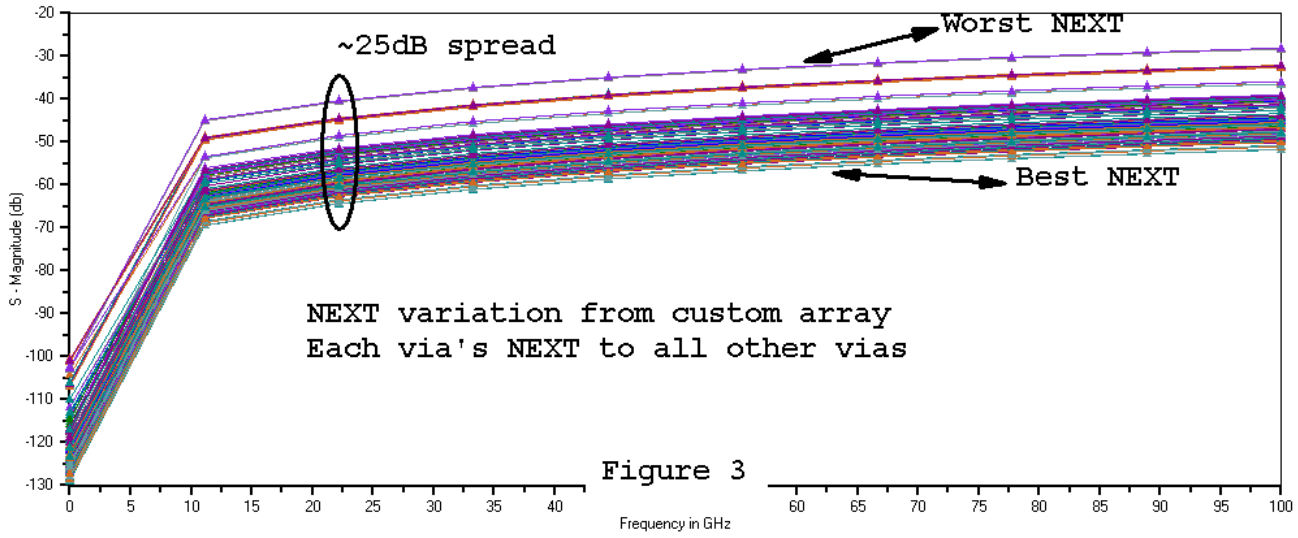


Figure 3

That is the beauty of path finding: objective data helps to compare different scenarios. For an in depth Full Wave EM solver discussion, please refer to Prof. Swaminathan's DesignCon2012 Tutorial[5].

The above analysis was restricted to silicon interposers (TSV) and could easily have been expanded to include glass interposers (TGV) to understand the benefits and costs between the two solutions[7].

Conclusion

Path Finding allows users a method to quickly analyze multiple solutions and choose the best one based upon: cost, performance (mechanical, thermal and electrical), area and power. Path Finding allows objective analysis to define how each design is constructed; it removes the folklore or 'gut' instincts based on historical results. 2.5D/3D technologies have existed for years; as shown in the above example, each variation is unique and must be analyzed. Path Finding methodology can accelerate the learning and reduce production risks; designing in reliability and costs effectiveness prior to physical verification or worst case on the production test floor.

2.5D/3D packaging technologies are revitalizing creativity in high technology products. We thought we knew what faster, better, lighter and smaller meant. 2.5D/3D packaging can revolutionize what we thought possible but it will require augmenting our current methods and tools. One key methodology to add would be Path Finding. Path Finding can ensure a design's structural integrity early in the development process and avoids finding issues that may be identified when it is too late to fix cheaply and quickly.

1. Challenger and O-Rings operating in temperatures well below tested scenarios or historical usage. http://en.wikipedia.org/wiki/Space_Shuttle_Challenger_disaster
   Picture: '" Space Shuttle "Challenger" explodes shortly after take-off.
2. Failure As A Design Criterion
   http://www.tech.plym.ac.uk/sme/Interactive_Resources/tutorials/FailureCases/hs1.html
3. "Been there, done that". Long ago, we allowed an authorized design center to implement a design from specification into an ASIC. When ASIC arrived, it did not work. As we identified the failure's root cause, we asked if this "component" was used elsewhere in the design. "Yes, ~18 times" was the answer. At that point, we realized a new design was required costing 6 calendar months, 12 engineering months and untold $'s. The respun ASIC worked like a champ.
4. Moongon Jung, Joydeep Mitra, David Z. Pan and Sung Kyu Lim, "TSV Stress-aware Full-Chip Mechanical Reliability Analysis and Optimization for 3D IC". DAC2011.
5. Madhavan Swaminathan, "Electrical Design and Modeling Challenges for 3D System Integration" DesignCon2012.
   http://www.e-systemdesign.com/pdfs/3DTutorialDesignCon2012.pdf
6. Tony Abbey article "Meshing for FEA". Desktop Engineering January 2013.
   http://www.deskeng.com/articles/aabhrs.htm

7. Madhavan Swaminathan interview with Francois van Trapp entitled:"The Flip Side of the Glass Interposer Coin". 3DinCites July 2012. http://www.infoneedle.com/posting/102426?snc=20641