**IFTLE 447 Micron and Rambus readying HBM2 products April 2020**

If we look back, almost a decade ago, 3D stacked memory was all the rage, and the leader in stacked memory development appeared to be Micron and their highly advertised memory cube which was announced at the 2011 Hot Chips Conference [link]. HMC featured a low-width bus & extremely high data rates to offer memory bandwidth that by far exceeded that of then standard DDR3.

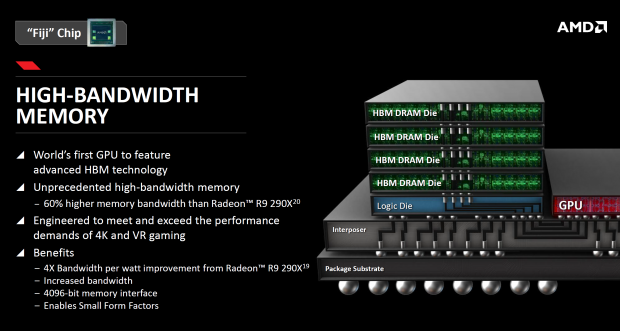
<https://ieeexplore.ieee.org/xpl/conhome/7470410/proceeding>

The first processor to use Micron HMCs was the [Fujitsu](https://en.wikipedia.org/wiki/Fujitsu) [SPARC64](https://en.wikipedia.org/wiki/SPARC64_V#SPARC64_XIfx) which was used in the [Fujitsu](https://en.wikipedia.org/wiki/Fujitsu) PRIMEHPC FX100 supercomputer introduced in 2015. There were also announcements in 2015 that Intel that was going to use the HMC in Knights Landing modules for high performance computing.



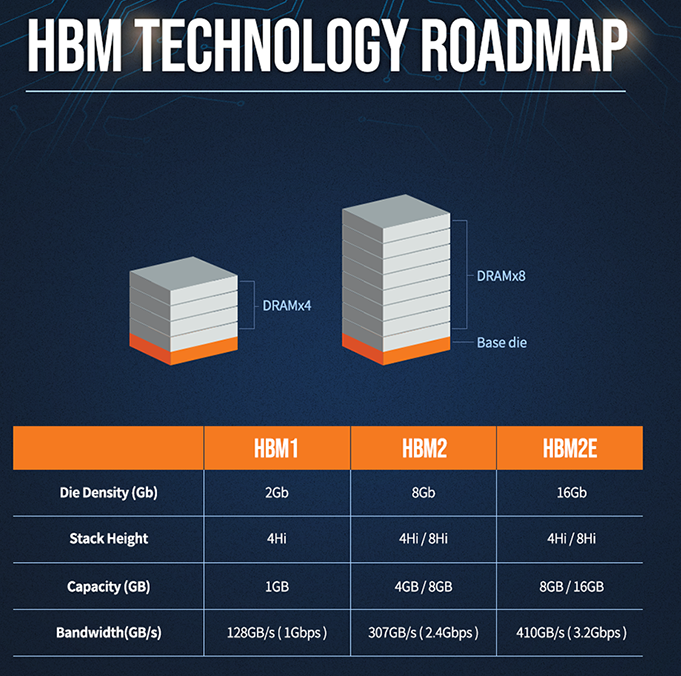
Intel Xeon Phi with HMC memory stacks [ca. 2015]

While Micron was working away on this program with their consortium that included IBM, Intel Altera, Xilinx, ARM, Samsung and SK Hynix, [HBM](https://www.amd.com/en/technologies/hbm)  was being developed within AMD / SK Hynix and was commercialized with the announcement of AMD's Fiji-based family of GPUs. Second generation product HBM2 first appeared in AMD's Vega GPUs.



Although Micron and HMC had a lead time of several years, AMD and partner SK Hynix were able to deliver a commercially accepted solution several years ahead of Micron. As Hynix launched the first generation of HBM and announced production of HBM2, Samsung, gave up waiting for HMC and switched to HBM production also.

HBM reduces the overall footprint memory devices by stacking memory cells onto the control logic die thus minimizing PCB real estate. Its wide bus structure reduces power consumption and delivers increased bandwidth.



By 2017 it was clear to all in the know that HBM was the clear market winner, and that Micron was not moving forward with their memory cube concept . The HMC consortium quietly faded away.

By the summer of 2018 Micron officially announced that their memory roadmap was changing [link]. In 2018, Micron announced the end of HMC and Intel cut off roadmaps with Xeon Phi, making it look like the end of this product line.

<https://www.micron.com/about/blog/2018/august/micron-announces-shift-in-high-performance-memory-roadmap-strategy>

In the last 5 years makers of GPUs and network processors have turned to HBM to meet their bandwidth needs. While HBM doesn’t yet generate high volume sales for Samsung or Hynix, it commands a price premium, which helps improve their profit margins.

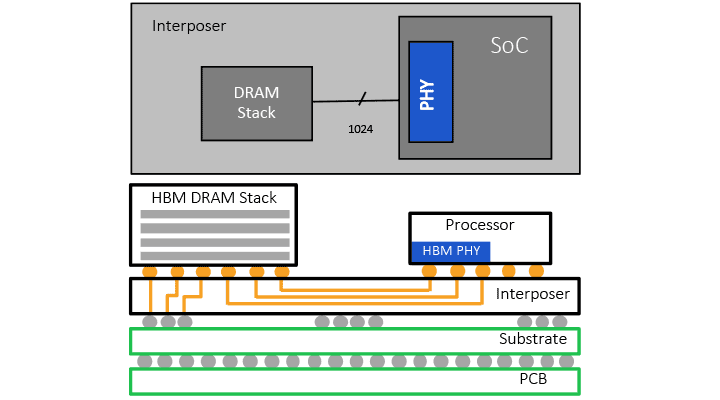
In 2019 Micron announced on their web page that “Micron has established an HBM development program”[link].

<https://www.micron.com/support/faqs>

Micron in their latest earnings report announced that later this year the company will finally introduce its first HBM2 DRAM, so we expect that by 2021 all 3 global memory manufacturers will be in the HBM market. Stacked HBM2 memory is expensive, but it is hoped that this additional competition will lead to reduced prices.

As another sign that HBM2 use is becoming more widespread, **Rambus** has announced new High Bandwidth Memory 2E (HBM2E) controller and physical layer (PHY) IP solutions [link] to enabling customers to integrate the HBM2E memory into their products. Rambus' controller and PHY design specifications meet JEDEC HBM2E standards.

<https://www.rambus.com/interface-ip/ddrn-phys/hbm/>



The Rambus design supports 12-high DRAM stacks of up to 24 Gb devices, or 36 GB of memory per 3D stack. This single 3D stack is capable of delivering 3.2 Gbps over a 1024-bit wide interface, delivering 410 GB/s of bandwidth per stack. The HBM2E controller core is DFI 3.1 and support logic interfaces like AXI and OCP.

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