THE X-RAY METROLOGY OF TSVS AND WAFER BUMPS

David Bernard, John Tingay, Philip Moyse, Simon White, Evstatin Krastev & Will Heeley
Nordson DAGE
Aylesbury, Buckinghamshire, U.K.
david.bernard@nordsondage.com

ABSTRACT
The emergence, development and use of Through Silicon Vias (TSVs) for the 2.5D and 3D integration of new products requires the availability of new inspection and measurement tools to validate TSV and 3D integration manufacturing procedures so as to ensure and optimise production yields and to provide high quality QA data. The areas where this need is most acute is in the measurement of the level of voiding that can be created during TSV fill, recognized as one of the major causes of poor yield in the TSV manufacturing process, and the level of voiding caused during the formation of wafer bumps. In particular, with TSV production most likely to be undertaken during the Middle End of Line (MEOL) or Back End of Line (BEOL) process flow, optical or infra-red techniques cannot provide this void data. Therefore, the use of x-rays offers a valuable, non-destructive method of inspecting and measuring TSVs and wafer bumps, not just for voiding, but also for a range of other critical dimensions.

Historically, x-ray inspection / measurement has not been available for use in these applications owing to the limitations of x-ray source resolution for the features of interest and the limited quantity of x-rays (or flux) that has been available to give fast data acquisition. However, this paper will present the results of non-destructive, on-wafer measurements of TSV voids, solder bump voids and other features using a new, production-ready x-ray metrology tool

Key words: Non-Destructive, X-ray Metrology, X-ray Inspection, TSV, wafer bump, Copper Pillar, Copper Pillar Alignment, Void, Voiding, Measurement, Critical Dimensions.

INTRODUCTION
The needs of being able to look inside an object without opening it up, or destroying it, and separating the different features within that would otherwise overlap each other when seen in a standard 2D x-ray image, are the same for the needs of electronics inspection on wafers and on printed circuit boards, as they are in the medical sphere. If there is a problem on a wafer (or a person!) ideally we want to analyse and measure the situation as much as possible, with everything in its natural, and existing, state before we opt, if necessary, to halt or modify a production process and / or take more radical action to probe the issues further with more invasive techniques and, possibly, a ‘surgical’, or destructive, inspection. If the fault / failure has been modified through an external analytical intervention then some important information might be lost from the subsequent analysis and thereby possibly obscure the root cause of the issue; for example, such as the need to modify process parameters.

The above reasons are why non-destructive 2D and 3D x-ray inspection has become, for many years, an important part of the inspection regime in electronics manufacturing, both for failure analysis and process development and control. Most recently, it has become even more important in printed circuit board (PCB) manufacture owing to the proliferation of devices that have optically hidden joints (such as BGAs, QFNs, POPs, MCMs, etc.) in addition to the needs of inspecting thru-hole joint quality and its assistance in identifying counterfeit components [1]. These inspection needs have been driven by the continuous shrinking of the optically-hidden feature sizes in electronic packages and the development of equipment by manufacturers of improved x-ray capabilities in terms of x-ray source, x-ray detector and sample manipulator geometry [1,2,3].

Traditionally, 2D x-ray inspection systems used for PCB applications can be seen as analogous to a simple 2D x-ray in the hospital. The only difference from a hospital environment is that the x-ray systems used for electronics inspection require that they provide magnification of the objects under test. However, the added complexity for electronics inspection is that you often have many different, varyingly-dense objects all within the same 3-dimensional volume - such as is typically found in a double-sided printed circuit board, or a complicated multi-layer package, for example, which means that the simple 2D x-ray image is often too cluttered with over-lapping features to allow for the easiest analysis. For PCB analysis, some of this over-lapping clutter can be removed by using oblique angle x-ray views of the sample. This can be achieved by tilting the sample with respect to the x-ray source to detector axis within the x-ray inspection system [2]. However, this method typically reduces the available magnification that can be achieved. This is why system manufacturers offer an alternative approach where the same result can be achieved by tilting the detector relative to the sample to achieve the oblique angle view, thus keeping the sample always in close proximity to the x-ray source, hence retaining the available geometric magnification [2].

Market Drive for Wafer Bump and TSV Measurement

The sizes of bumps used on wafers and for packages continue to shrink so as to provide greater I/O functionality within the same form factor. Bumps and copper pillar joints down to 25 µm, and below, in diameter are already well established.

The advent, and likely proliferation, of TSVs further extends this capability for more functionality & flexibility per package size and better, faster performance by providing closer connections between die and using less power to do so, thus, for example, offering longer battery life in mobile / portable electronics. This is achieved by using the TSVs as pathways through each die which can then be connected to other die above and below, if required. This approach may be able to maintain, in a more straightforward manner, 'More than Moore' scaling on transistor densities per die instead of, or delay migration to, smaller processing nodes and / or a move to 450 mm wafers. For example, TSVs allow for the creation of a mixed-mode processor + memory configuration in a single, vertically-stacked package and other multi-chip modules become viable within a small footprint. However, the full utilisation of TSVs in the next generation of packages will have to be justified in terms of performance improvements and not in terms of cost reduction. This is because the space on the die taken up with the TSVs cannot be used for processing, thus requiring a larger die area overall for each chip. As the manufacturing costs are essentially scaled by area of silicon covered / used, it means that implementing a TSV solution is not a low cost approach. To potentially offset this issue, consideration could be given to splitting up the functionality of more complicated large single die into multiple smaller individual die that can then be stacked and 're-integrated' into the full performance of the large die.

There are two methods of TSV utilisation today. Either 3D packaging, where there is complete 3D vertical stacking of multiple silicon die and the TSVs provide the architectural signal pathways between the dies and the package. Or 2.5D packaging, where individual die are not stacked on top of each other but sit adjacent to each other, connected by TSVs, onto a common carrier or 'backplane' that houses the necessary re-distribution layers to re-connect the functionality between the smaller individual die. This carrier is called an interposer and can be fabricated from silicon or glass and the TSVs are located in a fan-out method to handle the increased I/Os of the final package.

Making TSVs and Wafer Bumps – Challenges / Issues

Wafer and flip chip bumps can either be formed with solder spheres being reflowed onto the pads of the die or by masked plating the different constituent materials of the bump onto the silicon and then reflowing this melange into the final bump. The manufacture of the TSVs appears to have settled as either a via-middle or via-last process in the production process. Once the TSVs have been made they then have to be filled with metal (typically copper or tungsten) to provide the conductive pathway after the plating and passivation of the side walls. Anecdotally, it appears that in the TSV manufacturing process there is a trade-off between the speed of the filling process and the likely potential formation of voids. With both of these types of interconnect, the presence or absence of voiding within the final feature is not visible optically or with infra-red techniques. Therefore, the uncertainty of the quality of the process remains untested using these traditionally available techniques. If there is voiding, or only a partial fill in the full depth of the TSV, then not only could this impair electrical performance of the connection but, and perhaps more seriously, future high temperature processing of the total device could result in outgassing of the voids into the surrounding area. For a wafer bump, this could cause eruption and transfer of solder material into the surroundings, potentially causing shorts with neighbouring bumps and surface contamination. These issues are also possible with voids trapped within the TSV. However, of additional concern is the fact that the TSV voids are located within a small feature buried in a thinned wafer, so the liberation of this trapped air volume during later processing steps has more limited methods to escape its surroundings (top and bottom of a deep 'well') and this can only give cause for concern about the potential stress that this might placed on the TSV and the surrounding silicon.

At present, for TSV voiding analysis a FIB-SEM tool can be used to selectively etch its way down a single TSV and then image the exposed result to check the voiding. However, not only does this take a long time to achieve, at the end you have only inspected one TSV on a wafer that is likely to contain many millions. Furthermore, you have had to physically destroy that one TSV to do it and, by extension, potentially destroyed one of the whole devices unless 'sacrificial' TSV elements are available or have been designed in. Alternatively, a high performance, off-line x-ray inspection system could be used to non-destructively image a very small number of locations on a wafer. Apart from the issues of wafer handling and subsequent cleaning after using one of these latter types of system – especially if the void inspection is needed early in the fab process as would be the case with via-middle production of TSVs – at the moment the best that can be produced is some images of a handful of locations with a few TSVs or bumps per location. Such limited inspection is justified because there is little else that can be done but also because of the limited time available in production plus the additional complexity of requiring a value judgement to be made by the local operator as to the quality of what is being seen in the image. Of course, this entire approach makes the assumption that these results are valid over the whole wafer. Some void measurements can be taken from the 2D x-ray images of the wafer bumps on these systems, with larger bumps being easier to analyse. But the smallest bumps / pillars used today provide limited capability for measurement as they require the use of higher magnification imaging to see such tiny features and this reduces the number of objects that can be seen in each field of view – thus limiting further the coverage that can be undertaken on each wafer, if only a

few inspection locations are all that can be afforded to be investigated. These limitations are further exacerbated for TSV investigations as a 'top-down' view of a TSV makes it almost impossible to see the low density voids through the high aspect ratio of the relatively dense solder depth of the TSV. Therefore, at the very least, an oblique angle view is required of the TSVs in order to look along its effective length and more easily see the density contrast between void and fill material. Although existing off-line x-ray systems are able to achieve high magnification oblique angle views, for reasons that will be discussed below, this leave little or no opportunity to make measurements of voiding levels.

Use of X-rays for TSVs and Wafer Bump Metrology

Optical and infra-red techniques cannot be used for void measurements as they are unable to see the voids. The use of x-rays, therefore, offers an optimal way to make these measurements (see image 1). However, existing off-line x-ray systems have very limited capabilities in terms of wafer handling and measurement throughput. In order to overcome these limitations for non-destructive, fast, accurate metrology and defect analysis, rather than just inspection, of wafer bumps and TSVs, it is not just the available x-ray system geometries and speed of operation that needs improvement, the x-ray source and the detector capabilities need also to be improved [3] – especially such that wafer bumps / copper pillars of 25 µm, or less, in diameter and TSVs of diameters less than 10 µm can not just be seen but have sufficient clarity to be imaged, and thereby automatically analysed and measured, for variations in their condition. In addition to the measurement of voiding, other critical dimensions of the bumps and TSVs are also able to be analysed with x-ray metrology, such as bump pitch and diameter and TSV dimensions, fill level and side wall angles.

An added benefit of using x-rays for wafer metrology is that not only can a 2D image be taken on the sample, whether 'top-down' or from an angled view, but also 3D or computerised tomography (CT) techniques can be applied to the analysis. Both techniques offer advantages for the metrology that needs to be performed. A 2D x-ray image has an infinite depth of field – so all layers (objects at depth) in the image are seen with equal clarity. This is quite different from optical tools and means there is no need to re-focus the image if an object, or feature, is moved relative to an equivalent optical (z-) depth of field, such as if there was warpage on the wafer / device / feature. Any movement of the feature in the z-direction with respect to the x-ray source when using x-rays changes the geometric magnification in the resultant image. The closer the sample is to the x-ray source (for a fixed source – detector distance) then the greater the magnification of that feature in the image. The reverse is equally true. As a result, should there be any warpage on the sample then, for example, the pitch of wafer bumps in the image will alter dependent on their position from the x-ray source. Therefore, by knowing the bump size and pitch for a particular wafer inspection task, an effective x-ray metrology tool can calculate out any warpage variation that might be present and so provide consistent measurement data anywhere on the wafer. The use of a vacuum chuck to hold the sample will mitigate some extremes of any sample warpage but an optimal x-ray metrology solution, by necessity, has to be able to correct for this issue and provide seamless, reliable data for any measurement location.

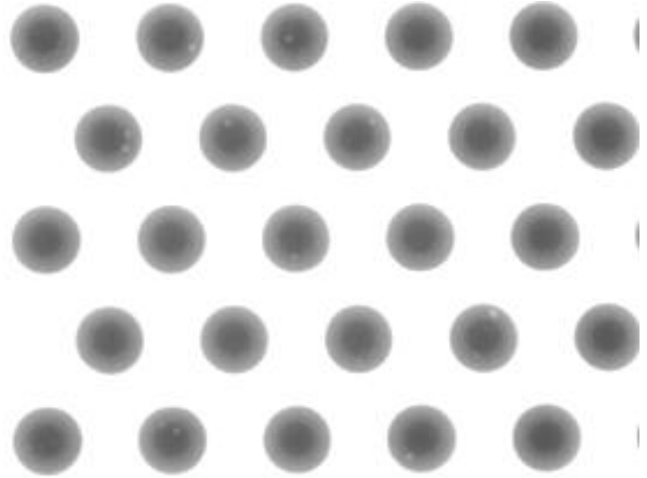

Image 1: X-ray image of 50 µm diameter wafer bumps. The lighter areas within the bumps are voids.

2D x-ray inspection offers the quickest solution for wafer bump void and critical dimension metrology when used with the right system geometry and manipulator speed and precision. However, for TSV metrology, the analysis of 2D x-ray images to provide measurements, even at oblique angle views, has some issues that therefore mean a 3D imaging solution is a better approach.

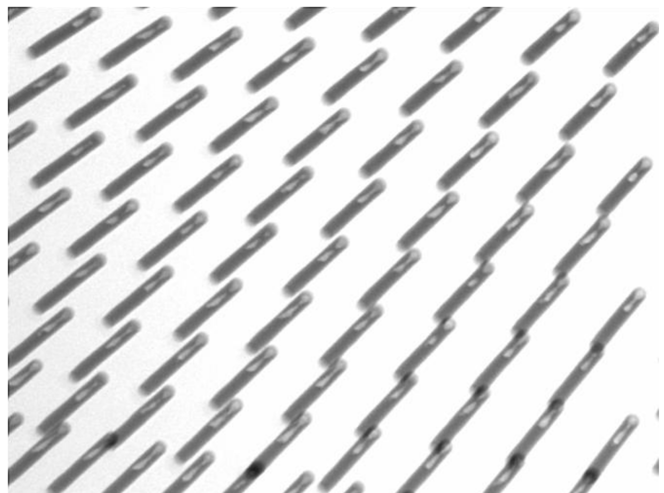

Image 2: Oblique view x-ray image of 10 x 100 µm TSVs. The lighter areas within the TSVs are voids.

Image 2 shows an oblique angled x-ray image of 10 x 100 µm filled TSVs. Although the presence of voiding in this case can be clearly seen such that an operator could make an expertise-based analysis of pass or fail, in this view you will notice that adjacent TSVs begin to overlap each other,

especially towards the edge of the image. This is caused by projection distortion in the image formed by having a point source of x-rays passing through and projecting the image of the TSV onto a large area detector. This has also been called 'gun-barrel' distortion where you can consider being able to look down the full length of the barrel (TSV) when it is placed in the centre of the image but as you move your point of view away from the centre then you can no longer see all the way down and, instead you see the 'outside' of the barrel with the angle of 'distortion' increasing as you move away from the centre. Although this is a well understood phenomenon, it means that if you are analysing the 2D x-ray image for metrology purposes then a problem arises as it becomes difficult, if not impossible, to see where one TSV starts and another ends (see image 2). Whilst this issue could be mitigated by only looking at those TSVs that do not overlap in the image, by necessity this would only be a very small portion in the centre of each image. If the pitch of the TSVs becomes smaller (as is likely) then this 'non-overlap' region in the image will also become smaller. Therefore, if you are only able to look at a small fraction of an image for analysis, it will dramatically increase the number of images that you will have to take to cover a representative meaningful number of TSV measurements on a wafer. This is not ideal. Instead, a better approach is to create a 3D model using CT techniques and then take measurement data from the 3D model.

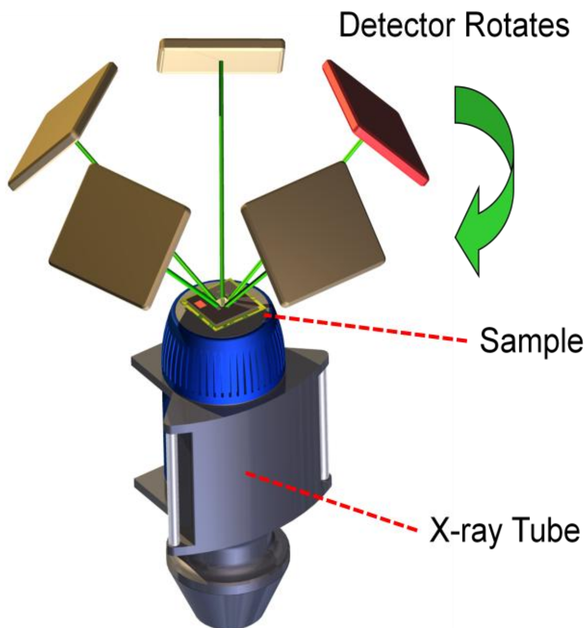

Figure 1. Schematic showing the concept of partial µCT where the detector moves at an angle around the area of inspection to obtain images from which the µCT reconstruction can be made.

The CT techniques that can be employed for TSV analysis are related to what would be might be familiar as a 'CAT' scan in a hospital that is used for diagnostic imaging. There are two CT approaches that could be used. Firstly, what is called full µCT and secondly what is called partial, or limited angle, µCT. More information on these techniques can be found in [1]. All CT techniques require a quantity of 2D x-ray images to be taken, or acquired, around the sample. Therefore more images must be taken to achieve the method than a single image that may be all that is necessary for 2D metrology. Once all the 2D x-ray images have been acquired, a mathematical reconstruction is applied to the set to re-create a 3D model of the sample based on density variation (see for example [4]). The 3D model is then available to be visualised or 'diced and sliced' at any re-constructed 2D plane within the model and from which analysis and measurement can be undertaken. The salient differences between the two methods for TSV applications can be considered as follows:

- Full µCT offers the best reconstructed model information in all 3 geometric directions (x, y and z). However, this technique requires images from all around the sample for best detail, typically achieved by rotation of the sample in between a fixed x-ray source and detector position. Taking many images around the sample will improve the quality of the final CT model but will take much longer to do. As the sample must be rotated, it has to be moved away from the x-ray source to prevent a collision during rotation. As the sample size increases, so the distance of the sample from the x-ray source must increase. This results in lower geometric magnification at the final image resulting in less detail in the final CT model. Overall, full µCT should be seen as destructive as only a very small sample can usually be used and the smaller the better so as to give better final resolution. Certainly nothing the size of a 300 mm wafer.
- Partial µCT captures the 2D x-ray images around the sample from the detector which is positioned at a fixed angle away from the 'top-down' view, see figure 1. This approach gives good reconstruction results in the z-direction (i.e. into the plane of the sample) but less good results compared to full µCT in x and y directions, owing to the lack of available information in the original 2D images that this geometry provides. However, this method is not limited with regard to sample size and so can be applied over any location in a large sample (such as a 300 mm wafer) and at the highest available magnifications, if required.

Therefore, to create a metrology system that will have the best throughput for inspecting TSVs in a production environment, partial µCT make the best sense. As an example, the top image of image 3 shows 3D rendered visualisation of some 10 x 100 µm TSVs that has been created with a partial µCT technique. The particular value of this approach for metrology purposes is shown by one of the reconstructed 2D slices in the lower image of image 3 that comes from a location part way down (in z) the depth of the three TSVs at the front of the upper image. Not only does the partial µCT approach indicate the presence or absence of voiding, together with its size, it is also able to indicate where in the depth of the device such features occur. This

allows additional metrology data to be captured from the same model and, perhaps most importantly, this method is not affected by any projection distortion allowing a larger image area to be reconstructed and analysed and no issues of being uncertain where one TSV starts and the other ends.

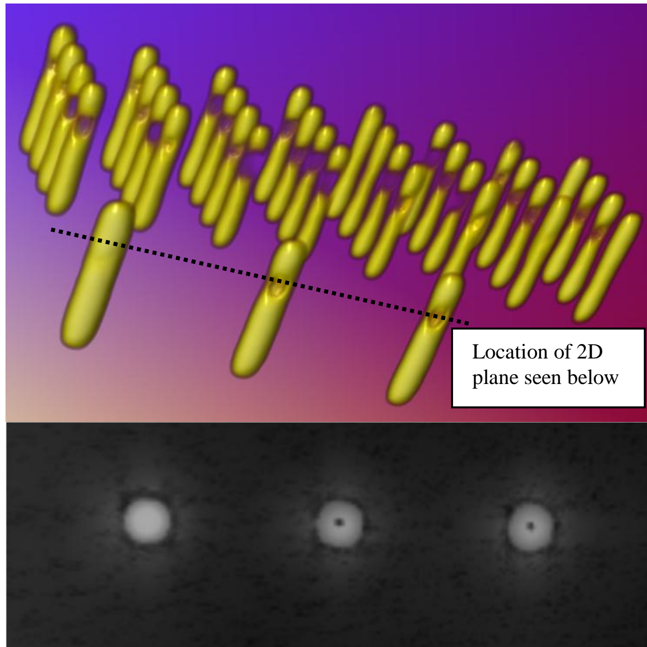

Image 3: Top image – 3D visualisation of 10 x 100 µm TSVs created with a partial µCT technique. Bottom image – reconstructed 2D slice from the 3D model ~ 1/3 the way down the 3 TSVs seen at the front of the top image. Voiding can be seen in two of the TSVs but not in he third at that level.

By having a 3D approach for TSV measurement and analysis, the same technique can also be applied for other applications, including what could be considered more complicated packages and devices, at least from an image analysis perspective, such as 3D ICs and MEMS devices. As all layers in these devices will be seen in the 2D image, 2D analysis will be more complicated than wafer bumps or TSVs. However, by creating a partial µCT model then different layers in the device can be highlighted for measurement and analysis with other layers and features removed from view. This technique could also be applied to wafer bumps if the position in z of the voids is required to assist with process development and improvement.

New Tool for TSV and Wafer Bump Metrology

The need for more non-destructive, high quality, fast, and automatic wafer bump and TSV metrology, as described above, is clear. Systems available in the market to date have limited, if any, capabilities to provide metrology and really only provide inspection – where an operator makes an informed judgment as to the outcome based on the image. Therefore, this paper introduces a new tool for automatic wafer x-ray metrology on up to 300 mm wafers in line with the demands detailed (see image 4). Depending on the application(s) required, the system can be configured for the optimum speed and throughput for the fastest 2D wafer bump measurements. Alternatively, it can be configured to provide measurements from both 2D and 3D (partial µCT) methods. In the latter configuration, 2D metrology on wafer bumps is still available but not at the same level of throughput as on the optimized ‘bump only’ arrangement. Replacement of the EFEM with alternative handler mechanisms opens up the configuration to package and MEMS analysis.

Image 4: XM8000 tool for TSV, wafer bump, 3D IC and MEMS metrology

RESULTS

300mm wafers containing different sizes of wafer bumps and TSVs have been evaluated in the XM8000 wafer x-ray metrology tool. The tool can be operated in 100% inspection mode (all bumps / TSV on all die). Alternatively, selected die and / or selected bumps or TSVs within a die can be chosen for analysis instead so as to improve throughput coverage. The maximum throughput that can be achieved depends on a number of factors, including but not limited to:

- Minimum void size that is to be detected (in % of the feature area or µm in diameter). This effectively defines the:
- Field of View (FOV) of each 2D x-ray image taken – i.e. how much area is covered by each image and this will therefore determine how many images will need to cover the required measurement area.
- Confidence level of correctly identifying each minimum void in each feature within each image. The greater the confidence level that is required to ensure identification of the minimum void selected then the smaller the FOV must be so as to have sufficient pixels covering the minimum void during analysis. To increase throughput therefore, consideration might be given to slightly reducing the confidence level for seeing the minimum void. This approach will enable a larger FOV to be used, and therefore provide quicker throughput, with the proviso of a slightly increased statistical risk of not seeing a particular minimum void. See figures 2 and 3.

- Die size and quantity of bumps / TSVs per die together with:
- Bump / TSV size, pitch and layout, as this impacts on the FOV required, the minimum void that might be identified and the number of images required to cover the desired area(s) of analysis.
- Having adequate density difference between the void and its surrounding material for sufficient contrast in the image to allow good measurement. It should be noted that as the bump or TSV increases in size then the physical size of the minimum void that can be realistically detected will also have to increase. This is because, for example, it is easier to see the density difference in the image of a small void on a small bump compared to the same void size on a much larger bump that contains substantially more dense material in the bulk of the feature.

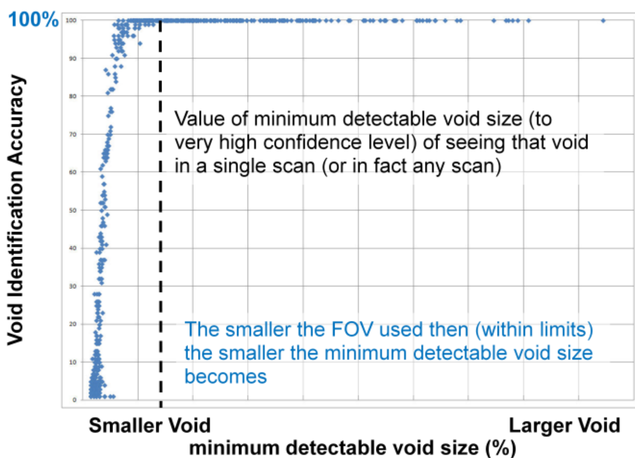

Figure 2: Void identification accuracy / confidence level as a function of FOV for a particular minimum detectable void setting.

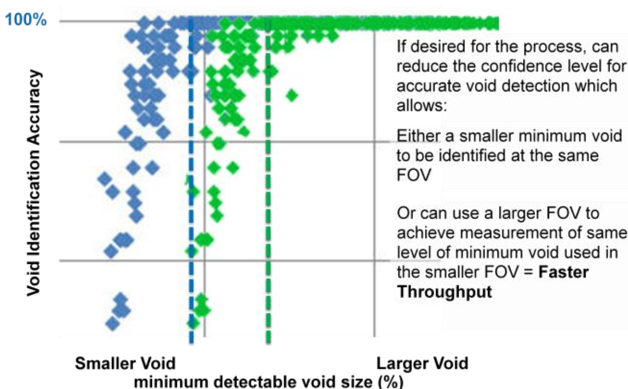

Figure 3: Effect of FOV, and therefore throughput improvement by considering altering the accuracy / confidence level acceptable for identifying the same minimum void size in a feature.

Throughput

Owing to the points mentioned above, throughput will be sample and test regime dependent. 100% inspection of 300mm wafers is available but optimal test deployment is likely to be best achieved with only partial analysis, as dictated by suitable process modelling, either on selected die and / or selected bumps within a die. Such an approach would provide throughput of wafers per hour.

Bench marking tests have indicated that for wafer bump metrology this new tool has up to 25 X the throughput of existing off-line systems. This allows a new paradigm of on-wafer metrology compared to existing procedures where a reasonable percentage (i.e. many thousands) of the bumps on the entire wafer can be measured in the same time that it takes with existing methods to measure as few as 5 locations per 300 mm wafer and only analysing < 50 bumps at each, giving a present coverage of only a few hundred bumps out of the whole wafer.

Further, publically available data will be provided at the conference presentation on bumps and TSVs.

CONCLUSION

A new x-ray tool has been developed to provide fast, non-destructive, automatic metrology for voiding and other critical dimensions on up to 300 mm wafers. It provides measurements in 2D and 3D modes to suit the requirements and the complexity of the sample.

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