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Electrical Design and Modeling Challenges for 3D System Integration

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Abstract

Over the last several years, the buzzword in the electronics industry has been "More than Moore", referring to the embedding of components into the package substrate and stacking of ICs and packages using wirebond and package on package (POP) technologies. This has led to the development of technologies that can lead to the ultra-miniaturization of electronic systems with coining of terms such as SIP (System in Package) and SOP (System on Package). More recently, the semiconductor industry has started focusing more on 3D integration using Through Silicon Vias (TSV). This is being quoted as a revolution in the electronics industry by several leading technologists. 3D technology, an alternative solution to the scaling problems being faced by the semiconductor industry provides a 3rd dimension for connecting transistors, ICs and packages together with short interconnections, with the possibility for miniaturization, as never before. The semiconductor industry is investing heavily on TSVs as it provides opportunities for improved performance, bandwidth, lower power, reduced delay, lower cost and overall system miniaturization. Interposers play a very important role in such 3D integrated systems since they act as the conduit for supplying power, interfacing to the external world and handling the thermal management for 3D IC stacks.
Two different technologies are being proposed for the interposer today namely, silicon and glass. Though glass provides a low loss substrate solution it has its disadvantages which can be corrected using silicon. Similarly, silicon has several performance advantages but is limited due to the semiconductor properties of the substrate which can be corrected using glass. So, which provides a better alternative from an electrical performance standpoint – silicon or glass?

In this paper, the electrical design and modeling challenges associated with 3D integration using TSVs is discussed with primary focus on the interposer. The results are contrasted with a glass interposer solution.

Author Biography

Madhavan Swaminathan received the B.E. degree in electronics and communication from the University of Madras, Chennai, India, and the M.S. and Ph.D. degrees in electrical engineering from Syracuse University, Syracuse, NY. He is currently the Joseph M. Pettit Professor in Electronics at the School of Electrical and Computer Engineering and the Director of the Interconnect and Packaging Center (IPC), an SRC Center of Excellence, at Georgia Tech, Atlanta. He was the Deputy Director of the Packaging Research Center, Georgia Tech, from 2004 to 2008. He is the Co-Founder of Jacket Micro Devices, a company specializing in integrated devices and modules for wireless applications(acquired by AVX Corporation) and the Founder of E-System Design, an EDA company focusing on CAD solutions for integrated microsystems, where he serves as the Chief Technical Officer. Prior to joining Georgia Tech, he was with the Advanced Packaging Laboratory, IBM, where he was involved in packaging for super computers. He is currently a Visiting Professor at Shanghai Jiao Tong University, Shanghai, China, and Thiagarajar Engineering College, Madurai, India. He has more than 350 publications in refereed journals and conferences, has coauthored three book

chapters, has 24 issued patents, and has several patents pending. While at IBM, he reached the second invention plateau. He is the author of the book Power Integrity Modeling and Design for Semiconductors and Systems (Englewood cliffs, NJ: Prentice-Hall, 2007) and the Co-Editor of the book Introduction to System on Package (SOP) (New York: McGraw Hill,2008). He has been selected by the IEEE EMC Society to serve as a Distinguished Lecturer for the 2012 – 2013 term. His research interests include mixed signal microsystem and nanosystem integration with emphasis on design, CAD, electrical test, thermal management, and new architectures.

1. Introduction

Through Silicon Via (TSV) is a new technology that provides short electrical connections between the top and bottom surface of a silicon substrate. When used in silicon stacking, TSVs provide short connections between transistors that are vertically separated from each other. The manner in which these connections are fabricated depend on whether via first, middle or last technology is used. In the area of packaging, TSVs used in silicon interposers also provide a short electrical path to the printed circuit board. What makes the modeling of TSVs interesting and its design challenging is the material properties of the medium surrounding these vertical interconnections. Due to the semi-conducting properties of the silicon medium; losses, capacitance effects and coupling behavior of TSVs are unique and are quite different for similar structures in a perfectly insulating medium. Hence, the electrical modeling of TSVs becomes important.

Silicon interposer technology is attractive since it enables the use of the existing semiconductor infrastructure for fabrication using earlier technology nodes. Since, the interposer does not contain any active devices and only contains passive interconnections, the interposers can be fabricated at a relatively lower cost. In addition, since the interposer has matched coefficient of thermal expansion (CTE) as compared to silicon, it acts as a buffer to relieve stresses between the chip stack and printed circuit board (PCB). However, due to the semiconducting properties of silicon, the vias and interconnections can create electrical design problems causing excessive coupling, which have been described in detail in this paper. Moreover, due to the multiscale dimensions of the interconnections used, extracting the parasitics of TSVs can be challenging depending on their density. To alleviate the electrical design problems associated with TSVs, alternate packaging solutions are being pursued such as the use of glass. The glass interposer solution is attractive since it provides very good insulating properties and can be fabricated in large panels, thereby potentially reducing the cost even further as compared to the silicon interposer. However, glass has a higher CTE as compared to silicon and has a thermal conductivity lower than silicon, causing hot spots, more so than silicon.

In this paper, the electrical design and modeling of TSVs used in interposers and in ICs (to a lesser extent) are discussed in detail followed by some results on the glass interposer. The two are then compared from a signal and power integrity standpoint, especially for high speed I/O signaling.

2. 3D Integration

2.A. Benefits of Through Silicon Vias

As is well known, TSVs provide short interconnection lengths as opposed to wirebond technology for stacking of ICs. Recent studies have shown that 3D DDR3 DRAM [Kang et al, 2010] can be enabled by using TSVs whereby 50% reduction in standby power and 25% reduction in active power is possible as compared to quad-die package with an increase in I/O speed from 1066Mbps to 1600Mbps. An emerging application is in the

area of wide I/O memory for mobile applications where logic and memory are being stacked on top of each other using TSV technology. In an interesting plenary talk given by Oh Hyun Kwon [ISSCC, 2010], he compared a conventional 3D package using Flip Chip Package on Package with LPDDR2 memory (low power DDR2) to an equivalent System in Package (SiP) with wide IO memory, as shown in Figure 1. Dramatic improvements in package size (35% reduction) and power consumption (50% reduction) were seen as shown in Figure 1(c). A very interesting aspect is the increase in bandwidth by 8X by supporting 512 I/Os transmitting at a data rate of 12.8Gbps as compared to 3.2Gbps in LPDDR2 memory.

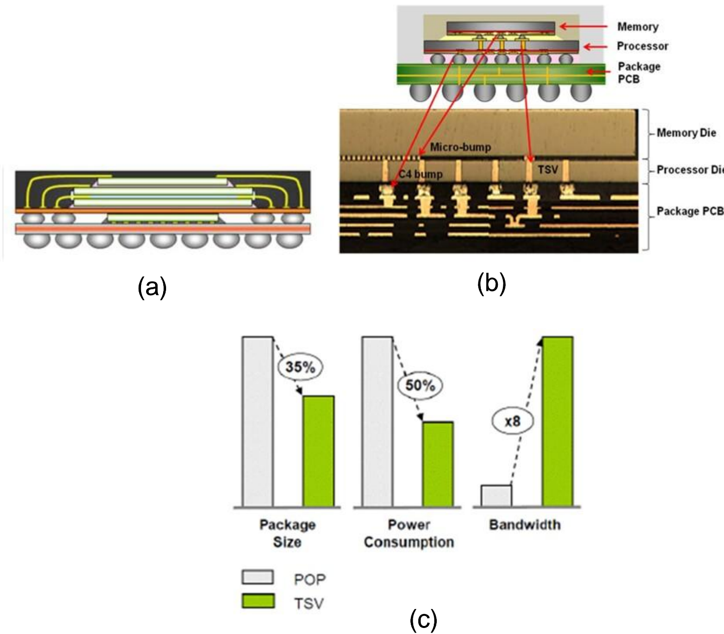


Figure 1: (a) FC-POP, (b) TSV-SiP with wide I/O DRAM an d (c) Performance Benefits

The reduction in package size is obvious since the wirebonds on the top tier in the memory stack in Figure 1(a) is around 1mm long, thereby using a large amount of area to package the memory stack as opposed to the flip chip processor in the bottom package. By replacing the wirebonds using TSVs in Figure 1(b), the interconnection length and therefore the package area can be reduced. The reduction in power can be attributed to the reduction in the capacitance of the TSV-SiP that needs to be charged and discharged as compared to the wirebond and routing capacitance in the FC-POP. Finally, the higher bandwidth for SiP-TSV is due to the fine pitch of the TSVs that provide more interconnections per unit area as compared to FC-POP, leading to 512 signal I/O connections (total connections is around 1200 including power and ground) between the processor and memory. Due to the shorter delay of TSVs due to the smaller interconnection length (1mm long wirebond as compared to 60μm long TSV), the speed of the processor-memory interface has increased from 3.2Gbps to 12.8Gbps. Clearly, the parasitics of the interconnections dictate to a large extent the electrical performance of either the FC-POP or TSV-SiP.

2.B. Integration Approaches

Currently three integration approaches are being pursued for system integration namely 1) 3D integration using chip stacking where the chips are interconnected to each other using TSVs and mounted on a silicon interposer or directly on a PCB, as shown in Figure 2 (a). The second approach is a 3D enabled approach where the silicon or glass interposer is used to connect chips to each other using TSVs or Through Glass Vias (TGV) as shown in Figure 2 (b). The third approach being touted as a 2.5D approach uses a silicon interposer with fine lines and vias to connect chips to each other, similar to a Multi-Chip Module which is then mounted on a PCB, as illustrated in Figure 2 (c). The solution in Figure 1(a) is currently being pursued by the mobile industry led by Samsung while Xilinx is pursuing the solution shown in Figure 2 (c) to reduce chip size (improves yield) and enable high throughput for FPGA based applications. The solution in Figure 2 (b) is currently at a research phase, with a lot of interest from system companies since it provides the ability to connect chips together without having to create TSVs in the logic chip, thereby providing more room for transistors and reducing stresses in the IC. The challenges in the electrical design aspects of the problem are similar for these integration approaches with some differences. Hence, the material presented in this paper should cover all these integration approaches.

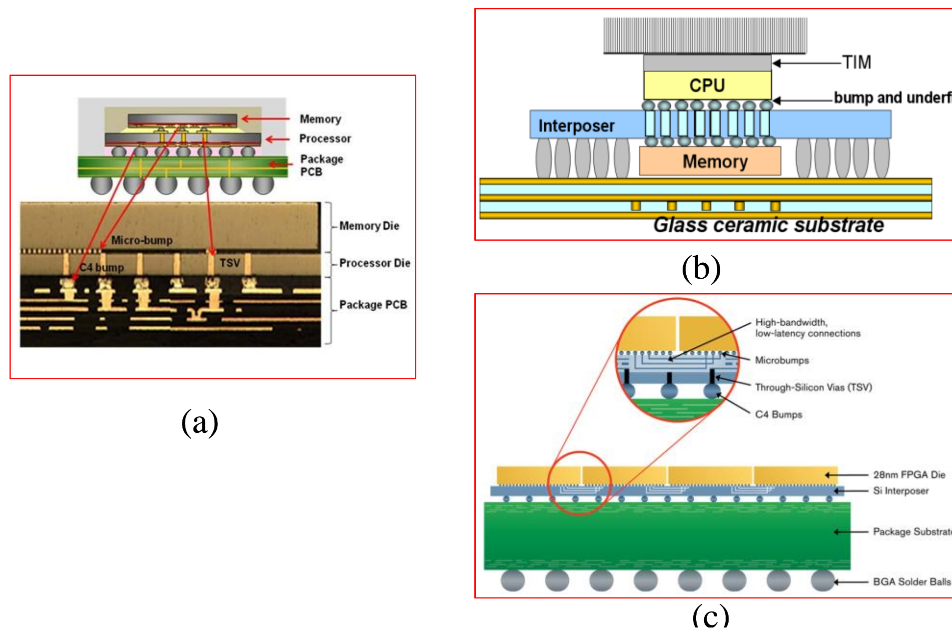


Figure 2: System Integration approaches (a) Chip stacking using TSVs on PCB (courtesy Samsung), (b) Interposer enabled 3D solution and (c) 2.5D solution using TSVs (courtesy Xilinx)

3. Electrical Modeling of Through Silicon Vias

3.A. Challenges

Consider a silicon stack as shown in Figure 3 (a) containing multiple tier, where each tier represents a die. The tiers are bonded to each other through microbumps or pads. Without loss of generality, the bottom most tier could be considered as the silicon interposer. The physical geometry associated with one of the tiers is enlarged in Figure 3 (b) showing the copper connections at the center of the TSV, surrounded by an oxide liner in a silicon medium. Depending on the process used, copper can be substituted with tungsten which provides a better Coefficient of Thermal Expansion (CTE) match to the silicon substrate but at the expense of higher resistance. The structure shown in Figure 3 (b) is also used in silicon interposers to package the stacked ICs. Two of the TSVs are shown in Figure 3 (c) to illustrate the physical geometry and material properties.

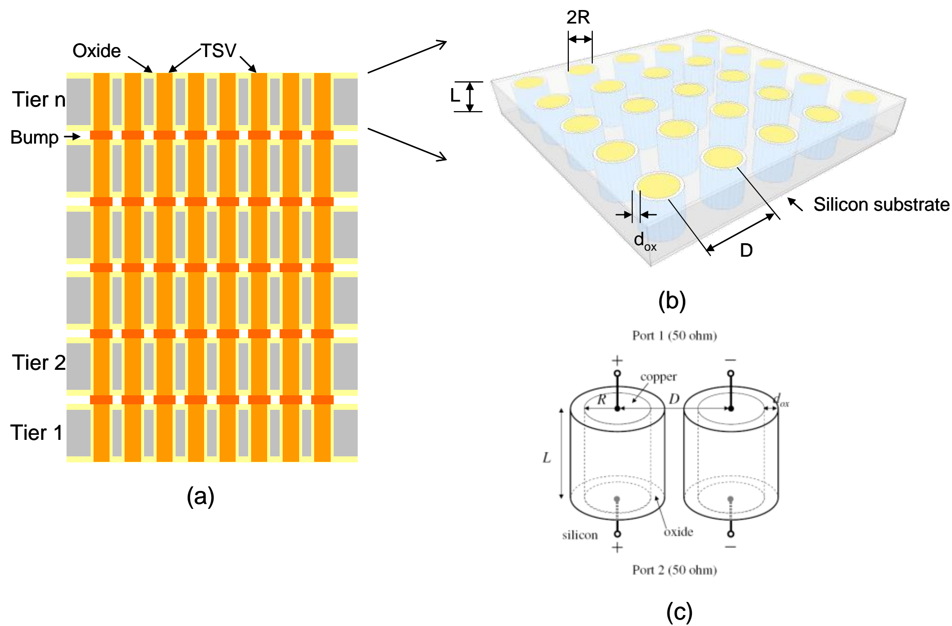


Figure 3: Through Silicon Vias (a) TSVs in 3D Stack with multiple chips (tiers), (b) TSV array in a tier and (c) Two TSVs

In Figure 3(c), each TSV consists of a metal center conductor of radius R (diameter D). The metal can either be copper (conductivity $\sigma = 5.8 \times 10^7$S/m) or tungsten (conductivity $\sigma = 1.9 \times 10^7$S/m). The center conductor is surrounded by an oxide (typically SiO_2) with a relative permittivity of 3.9. The metal conductor with oxide liner is embedded in a silicon based semi-conductor medium with relative permittivity of 11.9. A very important electrical parameter of the silicon medium is its conductivity which depends on the doping used. Standard CMOS grade silicon has a conductivity of 10S/m with high resistivity silicon having conductivity in the rage of 0.01S/m. In Figure 3(c), the ports (points of excitation and measurement) connected to the TSVs are referenced to 50 ohms for computing the scattering parameters. Typical dimensions for the TSVs are: diameter

(2R) in the range of 1.6-50μm, pitch D in the range of 2.4 – 80μm and length L in the range of 6 – 250μm. The oxide thickness d_{ox} is typically around 100 – 200nm depending on the process.

The extraction of the electrical parasitics of TSVs can be a challenging task for the following reasons: 1) the dimensions are multi-scale with an aspect ratio of 20:1 (L/2R) and oxide thickness of 100 – 200nm (d_{ox}), 2) it is embedded in a semiconducting medium which is lossy (CMOS grade silicon) making the electromagnetic wave propagation effects complex, 3) with TSV densities being greater than $10^5/cm^2$, the conductance and capacitance of the silicon substrate can cause significant leakage and coupling between TSVs, 4) biasing of the silicon substrate can change the TSV capacitance due to Metal-Oxide-Semidonductor capacitance behavior, 5) with temperature dependent conductivity, the resistance and conductance of TSVs become temperature dependent and 6) the electrical parameters are strongly frequency dependent. Due to these effects, with some being local and others global, arrays of TSVs have to be modeled (especially for interposers) in parallel making the problem a very complex one from a computational standpoint. Since, most electromagnetic solvers use a meshing scheme to discretize Maxwell's equations, it severely limits the number of TSVs that can be analyzed due to the multi-scale dimensions of the structures and the large number of TSVs that need to be analyzed. To approach this problem from a practical standpoint, two methods for computing the electrical parasitics of TSVs are described both of which do not require a mesh. These are 1) a physical model based approach using analytical equations and 2) a rigorous electromagnetic analysis based approach by solving Maxwell's equations using specialized basis functions that approximate the current and charge in TSVs without requiring a mesh.

3.B. Propagating Modes in Through Silicon Vias

A microstrip line on a semiconductor substrate such as Si (silicon) separated by SiO_2 (silicon-di-oxide) supports three fundamental modes of propagation namely, slow-wave, quasi-TEM and skin-effect modes. These modes have been discussed elegantly in [Hasegawa et al, 1971]. The three modes are separated based on the frequency, thickness of the SiO_2 layer, thickness of the Si substrate and silicon conductivity. Since, the TSV structure is similar to the microstrip line described by [Hasegawa et al, 1971] with a metal-SiO_2-Si interface, a similar set of propagating modes can be expected, which is described in this section.

Consider a signal and ground (return) TSV shown in Figure 4. The cylindrical copper conductor is surrounded by SiO_2 liner of thickness b1. The region between the two oxide liners contains the silicon substrate of thickness b2. Based on [Hasegawa et al, 1971], when the product of frequency and resistivity of the silicon substrate is large enough to produce a small dielectric loss angle, then the silicon substrate acts like a dielectric. In such a case the wave propagates in the presence of two dielectrics (SiO_2 and Si) between the signal and ground TSV and the fundamental mode is a quasi-TEM mode where the velocity of the wave is governed by the permittivity of the silicon substrate. The skin effect mode occurs when the product of substrate conductivity and frequency is large enough where the electric and magnetic fields have a small depth of penetration into silicon. In such a scenario, the silicon substrate acts as a conductor wall and appears as a

lossy ground plane to the signal conductor. The minimum frequency at which this occurs is when the skin depth $\delta = b_2$ (since $b_1 << b_2$). Since $\delta = \frac{1}{\sqrt{\pi f \mu \sigma_{Si}}}$ where $\mu = \mu_0$ is the permeability of free space and σ_{Si} is the conductivity of silicon, the frequency at which skin effect mode begins is $f = \frac{1}{\pi \mu \sigma_{Si} b_2^2}$. With typical silicon substrate conductivity of 10 S/m and $b_2 < 50\mu m$, the onset of skin effect mode occurs at high frequency when $f > 10^{12}$ Hz and is therefore not considered here. In addition to the dielectric and skin effect modes, a third mode called the "slow wave mode" can exist when the frequency is not high and the conductivity of the silicon substrate is moderate. This mode is a surface wave that occurs due to the strong interfacial polarization across the SiO_2 liner and has a velocity of propagation much slower than the silicon substrate due to the Maxwell-Wagner effect that increases the effective permittivity at lower frequencies [Hasegawa et al, 1971]. Given the frequency range of interest for most applications from DC to 100GHz and the typical dimensions of TSVs, the modes to consider for signal propagation are the slow wave and dielectric modes, which are discussed further in this section.

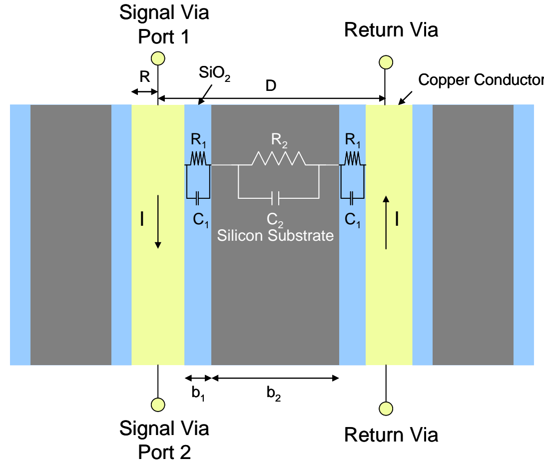


Figure 4: Signal and Ground TSV pair

The behavior of the slow wave and dielectric mode can be explained by the Maxwell-Wagner effect which is an interfacial relaxation process that occurs in all systems where the electric current must pass an interface between two dielectrics [Barlea et al, 2008]. The dispersion of the dielectric occurs in TSVs due to the series connection of the dielectric slabs formed by SiO_2 and Si. When the SiO_2 and Si dielectric layers can each be represented as a circuit with conductance and capacitance in parallel, connected to each other in series, then the interface can be charged by the conductance. This equivalent circuit representation and connectivity of the interfaces is shown in Figure 4, where R_1, C_1 and R_2, C_2 are the resistance and capacitance of the SiO_2 and Si substrate, respectively. The admittance of the three dielectric layers in series can be written as [Barlea et al, 2008]:

$$Y=\frac{\frac{R_1}{1+\omega^2\tau_1^2}+\frac{R_2}{1+\omega^2\tau_2^2}+\frac{R_1}{1+\omega^2\tau_1^2}+j\omega\left[\frac{\tau_1R_1}{1+\omega^2\tau_1^2}+\frac{\tau_2R_2}{1+\omega^2\tau_2^2}+\frac{\tau_1R_1}{1+\omega^2\tau_1^2}\right]}{\left[\frac{R_1}{1+\omega^2\tau_1^2}+\frac{R_2}{1+\omega^2\tau_2^2}+\frac{R_1}{1+\omega^2\tau_1^2}\right]^2+\omega^2\left[\frac{\tau_1R_1}{1+\omega^2\tau_1^2}+\frac{\tau_2R_2}{1+\omega^2\tau_2^2}+\frac{\tau_1R_1}{1+\omega^2\tau_1^2}\right]^2} \quad (1)$$

where 'ω' is the angular frequency and $\tau_i=R_iC_i$ i=1,2 is the time constant. The equivalent capacitance 'C' and conductance 'G' can be calculated as:

$$C=\frac{\mathrm{Im}(Y)}{\omega};G=\mathrm{Re}\,al(Y) \quad (2)$$

The capacitance C_1 of the oxide can be calculated approximately assuming a coaxial cable representation with inner radius 'R' and outer radius 'R+b1' as:

$$C_1=\frac{2\pi\varepsilon_{SiO_2}L}{\ln((R+b_1)/R)} \quad (3)$$

where 'L' is the length and ε_{SiO_2} is the permittivity of the oxide. For a TSV with L=100μm, R=15μm, b_1=0.1μm and using a relative permittivity of 3.9 for SiO_2, the capacitance C_1 can be calculated as 3.26pF. The capacitance C_2 can be calculated approximately assuming a two wire transmission line as:

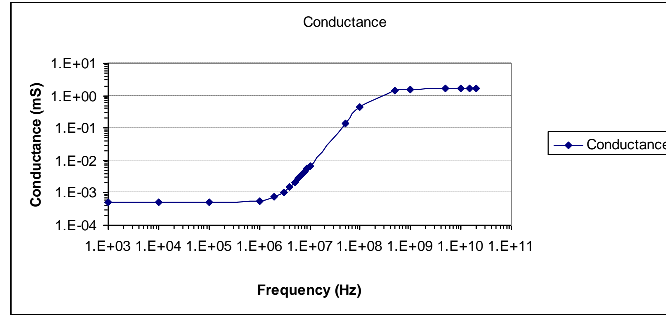
$$C_2=\frac{\pi\varepsilon_{Si}L}{\ln\left(\frac{D}{2R}+\sqrt{\frac{D^2}{4R^2}-1}\right)} \quad (4)$$

where 'D' is the pitch and ε_{Si} is the permittivity of the silicon substrate (since $b_1 << b_2$) . For a TSV with L=100μm, R=15μm, D=100μm and using a relative permittivity of 11.9 for silicon, the capacitance C_2 can be calculated as 0.0176pF. The conductance of SiO_2 is typically small since it is a good insulator and therefore its resistance R_1 is large, which is assumed to be 1MΩ. However, since the conductivity of the silicon substrate is large (10S/m), the resistance R_2 is much smaller than R_1. For a parallel RC circuit in the silicon substrate, the dissipation factor or loss tangent can be defined as $\tan d=\frac{G}{\omega C}$. In a dielectric, the loss tangent can also be computed as $\tan d=\frac{\sigma}{\omega\varepsilon'}$, where σ is the conductivity and 'ε' is the real part of permittivity. Therefore, the conductance of the silicon substrate can be computed as:

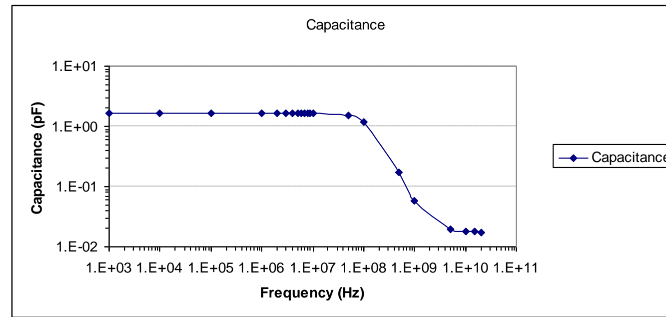
$$G_2=\frac{1}{R_2}=\frac{\pi\sigma_{Si}L}{\ln(\frac{D}{2R}+\sqrt{\frac{D^2}{4R^2}-1}} \quad (5)$$

Using (5), for the dimensions described, the resistance R_2 can be computed as 596Ω. With the defined parameters, the effective conductance and capacitance of the signal

TSV with respect to the ground TSV has been plotted in Figure 5 using equations (1) and (2).



(a)



(b)

Figure 5: Frequency Behavior (a) Effective Conductance and (b) Effective Cap acitance

Both the conductance and capacitance versus frequency curves in Figure 5 exhibit the classic Debye dispersion behavior. At low frequencies, $\omega \to 0$ and the time constant $\omega\tau_i << 1$. Therefore, the conductance G and capacitance C from equation (1) and (2) can be approximated as:

$$G = \frac{1}{2R_1 + R_2} = 0.5x10^{-3}\,mS$$
$$C = \frac{2R_1^2 C_1 + R_2^2 C_2}{(2R_1 + R_2)^2} = 1.63\,pF \qquad (6)$$

Hence, at low frequencies, the capacitance is large and the conductance small. Comparing with the capacitance of the two wire line from equation (4) which is 0.0176pF where the wave propagates in the silicon substrate with relative permittivity of 11.9, the capacitance at low frequencies is 92 times larger, indicating an effective permittivity of 1094 for wave propagation. This is the reason why at low frequencies, the TSV supports the propagation of a slow wave. It is important to note that the conductance (or leakage) of the slow wave is small, indicating that the wave attenuation is minimum at low frequencies (f<0.1MHz). At high frequencies, $\omega \to \infty$ and $\omega\tau_i >> 1$. In such a scenario, the conductance and capacitance from equations (1) and (2) can be approximated as:

$$G = \frac{2R_2C_2^2 + R_1C_1^2}{R_1R_2(2C_2 + C_1)^2} = 1.64mS$$
$$C = \frac{C_1C_2}{C_1 + 2C_2} = 0.0174pF \qquad (6)$$

Here, the conductance and capacitance are dictated by the material properties of the silicon substrate indicating that the silicon is acting as a lossy dielectric material. Here, the wave propagation is in the dielectric region between the two TSVs and is a quasi-TEM mode where the loss arises due to the displacement current. A question that often arises is, when does wave transition from a slow wave to a quasi-TEM mode. This can be explained using the discussion in [Hasegawa et al, 1971] by plotting the loss tangent given by $\tan d = \frac{\omega C}{G}$ for an equivalent series RC circuit.

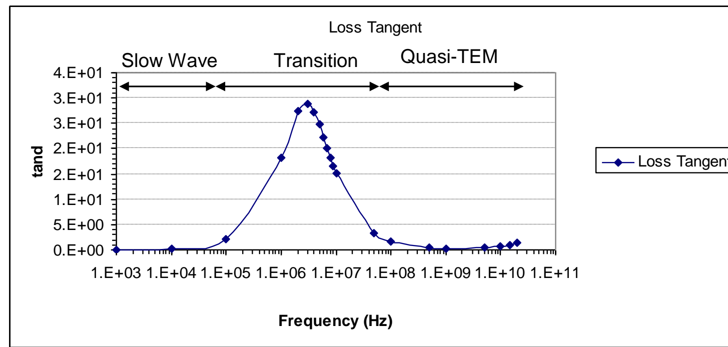


Figure 6: Loss tangent Vs Frequency

In Figure 6, the variation of the loss tangent with frequency is shown where the loss tangent is small at low frequencies, reaches a maximum at around 3MHz and then decreases to a low value beyond 0.5GHz. The frequency at which the maxima occurs for the loss tangent is the transition frequency where the slow wave mode transitions into a diffusion type TEM mode followed by a quasi-TEM mode. During the transition phase between the slow wave to the quasi-TEM mode (0.1MHz - .5GHz), the attenuation increases significantly per wavelength, followed by a reduction in the loss per wavelength at frequencies beyond 0.5GHz. Such a behavior will not be seen if a good insulator is used instead of Si (conductivity of ~$1\text{x}10^{-7}$ S/m) since the insulator will behave like a dielectric supporting only the quasi-TEM mode.

3.C. Physics Based Modeling of Through Silicon Vias

In the previous section approximate equations were derived for the oxide capacitance, substrate capacitance and substrate conductance between a signal and ground TSV. This captures the insulating and semiconductor behavior of the dielectric material used. These equations were derived based on the physics associated with the wave propagation in a coaxial transmission line and a two wire line. A similar approach can be used to compute the inductance and the resistance of the conductors due to current flowing through them.

A two wire model can be used to compute the loop inductance L_{ind} of two TSVs as [Kim et al, 2011]:

$$L_{ind} = \frac{\mu_0 \mu_r}{2\pi} \ln(\frac{D}{R}) L \qquad (7)$$

where μ_0 is the permeability of free space and $\mu_r = 1$ is the relative permeability of the substrate. From Figure 3, setting D = 100µm, L=100µm and R=15µm, the loop inductance can be computed as 37.9pH. Two effects that are not captured in (7) is the frequency dependence of inductance due to skin effect and proximity effect due to current flowing on neighboring conductors. For TSVs, the frequency dependent variation of inductance is small and can be neglected. However, the proximity effect which is due to the non-uniform distribution of current in the conductor due to neighboring conductors can have a large effect on the inductance, which is not captured in (7). In [Kim et al, 2011], a proximity factor has been used to modify (7) based on the ratio of pitch (D) to diameter (2R) of the TSVs. Later in this paper, the proximity effect is discussed in more detail based on rigorous electromagnetic analysis. For now, let's use (7) to calculate the loop inductance of the TSV pair. Based on [Kim et al, 2011], the resistance variation with frequency can be computed using:

$$R = \sqrt{R_{dc}^2 + R_{ac}^2}$$
$$R_{dc} = \frac{1}{\sigma_{Cu}} \times \frac{L}{\pi R^2}; R_{ac} = \frac{1}{\sigma_{Cu}} \times \frac{L}{\pi \left[R^2 - (R-\delta)^2\right]} \qquad (8)$$
$$\delta = \frac{1}{\sqrt{\pi f \mu_0 \sigma_{Cu}}}$$

where δ is the skin depth, σ_{Cu} is the conductivity of copper (5.8 x 10^7 S/m), μ_0 is the permeability of free space, R_{dc} is the DC resistance, R_{ac} is the ac resistance and the other physical parameters are defined as shown in Figure 3. The variation of resistance with frequency for L=100µm and R=15µm is shown in Figure 7 where the resistance increases from 2.44 mohms at low frequency to 39.84 mohms at 20GHz.

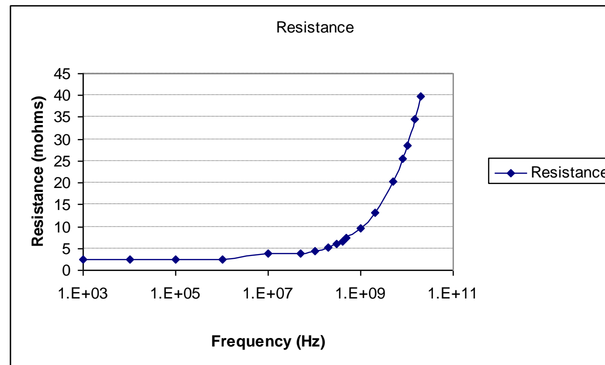


Figure 7: Resistance Vs Frequency

It is important to note that the resistance shown in Figure 7 is for a single TSV. For a pair of TSVs (signal and ground as in Figure 3), the resistance doubles.

3.D. Equivalent Circuit and S-Parameters for TSV pair

Using the computed R, L, G, C parameters, an equivalent circuit for a differential TSV pair (signal TSV with reference supporting current in opposite directions as shown) can be constructed as shown in Figure 8 (a). This equivalent circuit is a lumped T-element circuit that is symmetric, where R, L are series elements and G, C are shunt elements. The parameters R, G, C are frequency dependent parameters as described earlier with L being frequency independent. The T-element circuit in Figure 8 (a) can be further simplified to the circuit shown in Figure 8 (b) where the impedance z and admittance y, which are frequency dependent parameters, can be computed as:

$$z(f) = 2R + j\omega L;\ y(f) = G + j\omega C \tag{9}$$

where G, C are the equivalent conductance and capacitance from (2) and ω is the angular frequency in rad/s.

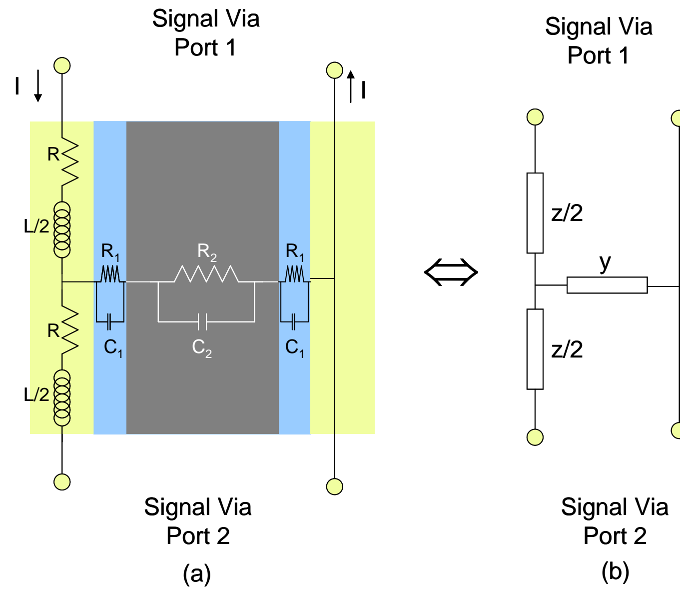


Figure 8: T Element equivalent circuit (a) R,L,G,C parameters and (b) Z,Y parameters

Based on the physical dimensions and material properties used to compute the R,L,G,C parameters (D=100µm, R=15µm, L=100µm, d_{ox}=0.1µm, ε_{SiO2}=3.9 and ε_{Si} = 11.9), using the T-element equivalent circuit in Figure 8 (b), the computed insertion loss S(1,2) (decibels) for the differential TSV pair is shown in Figure 9 as 'o' (Physics) from 1KHz to 20GHz (return loss S(1,1) not shown). The correlation of the physics based model to electromagnetic simulations (shown as line and explained later) is quite good with a small deviation at higher frequencies. From the figure, the sharp slope associated with the insertion loss up to ~0.5GHz can be seen due to the transition from the slow wave to the quasi-TEM mode described earlier. After around 0.5GHz, the slope of the curve

decreases indicating that the displacement currents in the silicon substrate begin to contribute towards the loss. Such a sharp increase in insertion loss up to ~0.5GHz will never be seen for vias passing through good insulators and is therefore unique to Through Silicon Vias. From Figure 9, an insertion loss of ~0.37dB at 20GHz is quite large considering that the length of the TSVs is just 100μm.

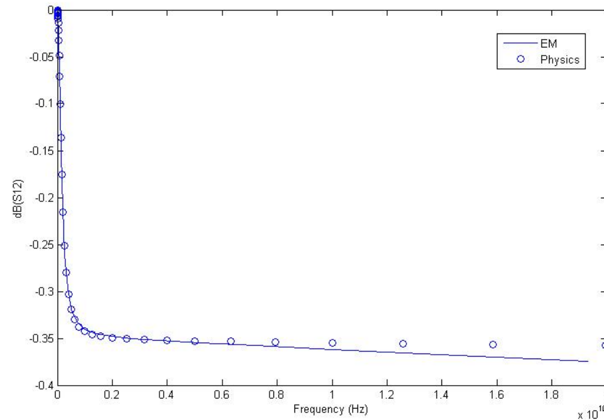


Figure 9: Insertion Loss of differential TSV

3.E. Rigorous Electromagnetic Modeling

In this section a full-wave 3D electromagnetic method is used to compute the response of through silicon via interconnections.

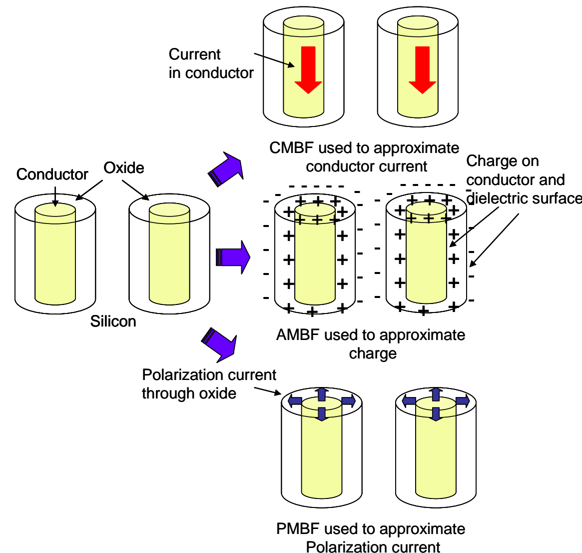


Figure 10: Electromagnetic modeling of TSVs using cylindrical basis functions

An important observation about TSV interconnections is that they have a circular cross section and a cylindrical structure. This property enables to derive specialized basis functions which approximate the current and charge in the TSVs. Using the basis functions, the electrical response of the structure can be extracted by solving Maxwell's equations. A TSV pair is shown in Figure 10, where the conduction current flows through the center conductor, charge is generated on the conductor and dielectric surfaces and polarization current flows through the oxide between the conductor and silicon substrate. By using specialized basis functions to approximate the current and charge, solving the appropriate Maxwell's equations, and calculating equivalent circuit parameters, an electrical equivalent circuit can be derived for the TSV pair, as described in [Han et al 2010]. This electrical circuit looks similar to Figure 8 with the difference that the conduction current, charge and polarization current are approximated by accounting for the non-uniformity of the current and charge (proximity effect) and by accounting for all the modal variations expected in an electromagnetic response. The frequency dependent RLGC parameters of TSVs through electromagnetic modeling can therefore be computed as follows [Han et al, 2010]:

a) Conductor series resistance and inductance: This represents the loss and inductive coupling in copper conductors, which are due to the volume current density distribution. The conductor series impedance in Figure 11 can be extracted by solving the electric field integral equation (EFIE) with cylindrical conduction mode basis functions (CMBF) [Han et al, 2010]. The circles in the equivalent circuit in Figure 11 is the contribution due to inductive coupling.

b) *Substrate parallel conductance and capacitance*: This represents the conductance and capacitance between conductor and infinite ground, between dielectric and infinite ground and between dielectrics in the substrate (Figure 11) produced by the surface charge density distribution on the conductor and dielectric surfaces. The parallel admittance can be extracted by solving scalar potential integral equation (SPIE) with cylindrical accumulation mode basis functions (AMBF). The conductance terms can be computed by using the complex permittivity for silicon defined as:

$$\varepsilon_{Si} = \varepsilon_0 \varepsilon_{Si,i} (1 - j \tan\delta - j \frac{\sigma_{Si}}{\omega \varepsilon_0 \varepsilon_{Si,i}}) \qquad (10)$$

where $\varepsilon_{Si,i} = 11.9$ is the relative permittivity of silicon, σ_{Si} is the conductivity of silicon based on the doping and $\tan\delta$ is the intrinsic loss tangent.

c) *Excess capacitance in oxide liner*: This represents the effect of the insulator between conductor and silicon substrate which originates from polarization current in the insulator. Unlike the conduction current which flows along a longitudinal direction, the polarization current flows radially, between the conductor and silicon substrate. To capture the polarization current density distribution, new basis functions are required in addition to CMBF and AMBF. These basis functions are called polarization mode basis functions (PMBF).

By solving for the RLGC elements that capture effects related to non-uniform charge and current density distribution in the TSVs due to proximity effect, the parasitics of TSVs can be extracted more accurately. As illustrated in Figure 10, the extracted individual elements are combined to generate the complete equivalent circuit model. A major

challenge arising with the modeling of TSVs are the multi-scale dimensions involved due to the thin oxide thickness, aspect ratio and the need for modeling multiple TSVs to extract coupling effects.

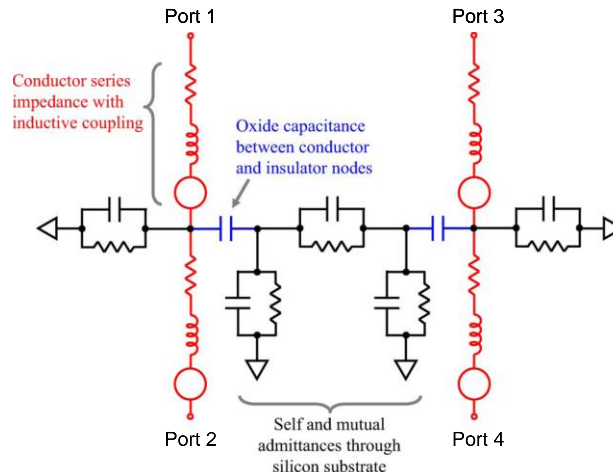


Figure 11: Derived equivalent circuit using specialized basis functions

This is due to the need for meshing the structure where many mesh elements may be required due to the multi-scale dimensions involved. Using specialized basis functions as described in this section eliminates the need for meshing and therefore the solution described is both memory efficient and computationally less expensive. In addition it is more accurate as compared to physics based modeling described earlier specially for TSV arrays where coupling needs to be captured accurately due to the non-uniform charge distribution arising due to proximity effects.

The result from the rigorous electromagnetic modeling technique has been compared with the physics based model in Figure 9 for a TSV pair. The results agree quite well. A fair question that needs to be answered is the following: If the simple physics based model provides a reasonably good accuracy as compared to the rigorous electromagnetic solution as shown in Figure 9, why then bother to develop such a sophisticated solution for analyzing TSVs. This is because the distribution of charge on the TSVs becomes non-uniform as the density and number of TSVs increases. This effect is compounded when non-uniform spacing between TSVs due to the presence of Keep Out Zones (regions without metal for managing mechanical stresses) further complicates the distribution of charge making it difficult to use simple analytical models. This effect, called as the proximity effect, is an important effect to capture during the modeling of TSVs to compute both insertion loss and coupling, which requires full wave electromagnetic analysis. Since the electromagnetic analysis described in this section is customized to solving TSVs with cylindrical cross section, it provides an advantage over other generic electromagnetic solvers in terms of accuracy, speed and memory utilization.

3.F. MOS Capacitance Effect

In all of the structures considered, the silicon substrate has been considered as a lossy material and its semiconductor properties have been ignored. These models ignore the

voltage-dependent MOS capacitance of the TSVs. In interposers, the substrate is often times not grounded and hence the MOS capacitance effect does not impact the response. However, in ICs, the substrate is biased and therefore the MOS capacitance results in a decrease in the total capacitance, which is a benefit since it reduces leakage into the silicon material.

Consider the TSV shown in Figure 12 (a) which consists of a cylindrical conductor surrounded by an oxide liner embedded in a silicon substrate with silicon di oxide (SiO_2) inter-layer dielectric (ILD) on either side. Such a TSV under bias conditions exhibits a capacitance behavior similar to a planar MOS capacitor, as shown in Figure 12 (b), where V_{FB} is the flat band voltage, V_T is the threshold voltage and V_g is the gate bias voltage.

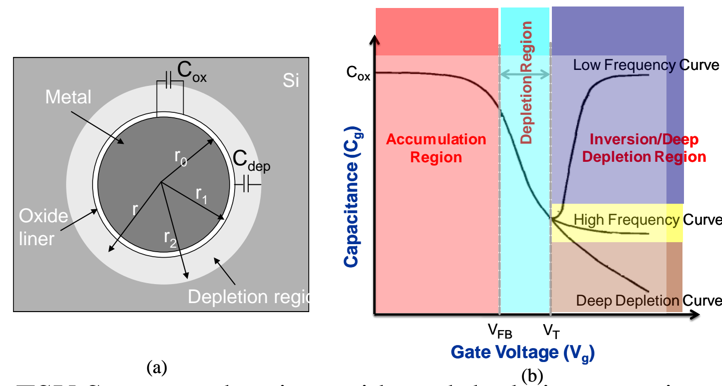


Figure 12: (a) TSV Structure showing oxide and depletion capacitance and (b) Capa citance voltage plot for planar MOS capacitor on p-type silicon

A behavior similar to Figure 12(b) is expected for a TSV as well where the capacitance between the conductor and silicon substrate equals the oxide capacitance in the accumulation region but decreases in the depletion, inversion and deep depletion regions and is based on the bias voltage (shown as gate voltage for a MOS capacitor in Figure 12 (b)). Beyond the threshold voltage V_T, three curves are shown which can be used to differentiate a signal TSV from power/ground TSVs, as explained in [Band et al, 2011]. When the DC component of the gate voltage changes very fast (~5V/ns), the generation of minority carriers cannot keep up with the rate of change of gate voltage. Hence no inversion region is formed around the oxide and any increase in the gate voltage is matched by an increase in the width of the depletion region. This occurs in signal TSVs where high frequency signals propagate and follows the deep depletion curve shown in Figure 12 (b). When the DC component of the gate voltage changes slowly, an inversion region is formed for high gate voltage. The MOS capacitance in this scenario is dictated by the small signal AC component of the gate voltage. When the AC signal contains high frequency components (~>1MHz), the minority carrier generation rate is unable to keep up with it, resulting in an increase in the depletion region as the gate voltage increases. This corresponds to the high frequency curve in Figure 12 (b) and occurs in power and ground TSVs containing high frequency noise signals. When the gate voltage has a low-frequency small-signal AC component, the minority carrier generation rate matches any change in the gate voltage, resulting in the inversion region width being proportional to the gate voltage. In such a situation, the low frequency curve in Figure 12 (b) results and occurs in the power and ground TSVs containing low frequency noise transients. In this

section, two methods have been used to extract this capacitance based on a full-depletion approximation (FDA) [Band et al, 2009; Katti et al, 2010] and rigorous numerical modeling [Band et al, 2011; Band, 2011]. The voltage-dependent MOS capacitance is then used to extract the frequency response of the TSVs.

As an example consider a copper TSV of radius 15μm, oxide thickness 0.1μm, length 100μm, oxide relative permittivity 3.9, silicon relative permittivity 11.9 and in a silicon substrate of conductivity 10 S/m (N_a=0.137 x 10^{22} /m^3). The variation of capacitance (C_{tot}) with bias voltage (V_{TSV}) is shown in Figure 13 (a), (b) and (c) using two methods namely, the Full Depletion Analysis (FDA) and numerical analysis for the low frequency, high frequency and deep depletion mode of operation. As a comparison, the oxide capacitance (C_{ox}) is also shown that neglects the biasing effect. From the figures it is clear that the oxide capacitance overestimates the signal capacitance to the substrate due to biasing.

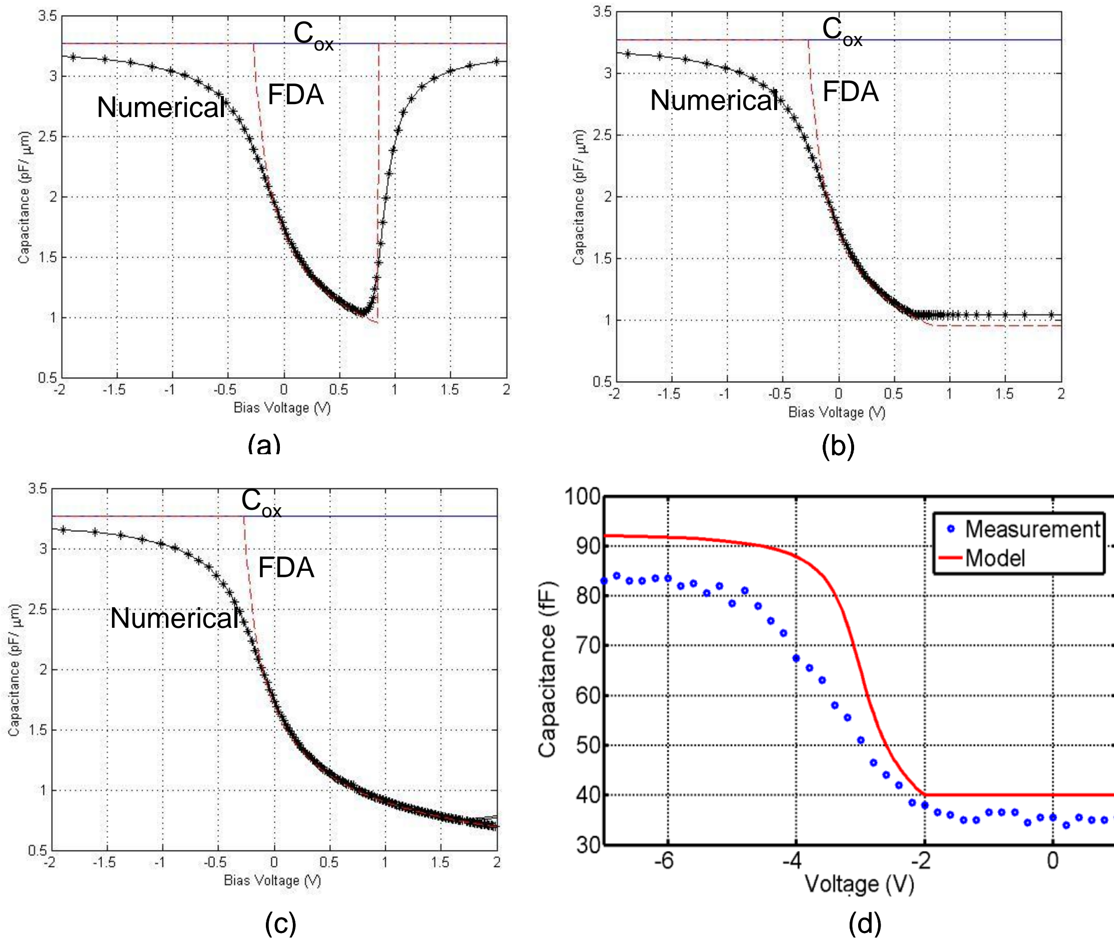


Figure 13: Capacitance Vs Bias Voltage (a) Low Frequency, (b) High Frequency, (c) Deep Depletion and (d) Model to Hardware correlation

In Figure 13 (a)-(c), even though FDA is inaccurate as compared to the numerical analysis, it provides a simple and quick way of estimating the capacitance for a given bias voltage. The accuracy of the numerical analysis is validated through measurements [Katti et al, 2010] in Figure 13 (d) for a TSV with 5 μm diameter, 20 μm length, copper metallization, SiO_2 oxide liner of thickness 118.2 nm and with a doping concentration of

the p-type Si substrate of $2x10^5$ cm^{-3}. The correlation is reasonably good given the limited information on the TSV parameters.

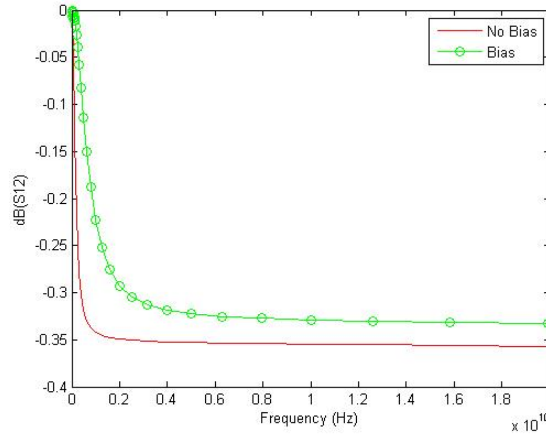


Figure 14: Insertion Loss with and without bias voltage

If the bias voltage reduces the signal capacitance to the substrate, then it should have an impact on the insertion loss of the signal. Consider a signal and ground return TSV shown in Figure 3 with D=100µm, R=15µm, L=100µ, d_{ox}=0.1µm, ε_{ox}=3.9 and ε_{Si} = 11.9 and biased at 1.8059V. From Figure 13 (c), the deep depletion curve results in a total capacitance (C_{tot}) of 0.7264pF. This is due to a depletion capacitance (C_{dep}) of 0.9343pF in series with the oxide capacitance (C_{ox}) of 3.2653pF. Using the model in Figure 8 and replacing C_1 with 0.7264pF, the insertion loss for a signal and ground return via referenced to 50Ω can be computed, which is shown in Figure 14 and compared to the case where the oxide capacitance of 3.2653pF is used for the capacitance C_1 (no bias). Clearly, with a lower bias capacitance, the insertion loss is lowered which results in a more gradual slope for the insertion loss during the slow wave to quasi-TEM transition phase.

4. Design Issues

The rigorous electromagnetic method described in section 3.E has been converted into a windows based modeling tool called Sphinx 3D Path Finder [Sphinx 3D Path Finder, 2011]. Since the electromagnetic modeling method described is not limited to two TSVs, this tool enables the modeling of large arrays of TSVs. In this section, TSVs will be analyzed for technology tuning and cross talk. In addition, a brief comparison between silicon and glass interposer will be provided.

4. A. Technology Tuning

Process optimization requires the variation of the physical parameters of the TSV geometry to understand its impact on the electrical response. Here, the insertion loss has been used as a measure to assess the impact of the physical parameters such as TSV length, oxide thickness and pitch. In Figure 15 (a), as the TSV length decreases, the insertion loss improves, which is desirable. Changing the oxide thickness only changes

the insertion loss in the transition region, as shown in Figure 15 (b). At higher frequencies, when the quasi-TEM mode propagates, the oxide thickness has little effect. Finally in 15 (c), the pitch has been varied. A reduction in pitch increases the insertion loss due to the reference to 50 ohms. Hence, a reduced pitch provides reduced matching. Depending on the application, the process parameters can be varied to obtain the optimum insertion loss. Though the insertion loss for TSVs is higher as compared to vias in a low loss dielectric, this increased insertion loss is not a major issue when connected to interconnections, as explained later. A larger issue is the coupling between the TSVs.

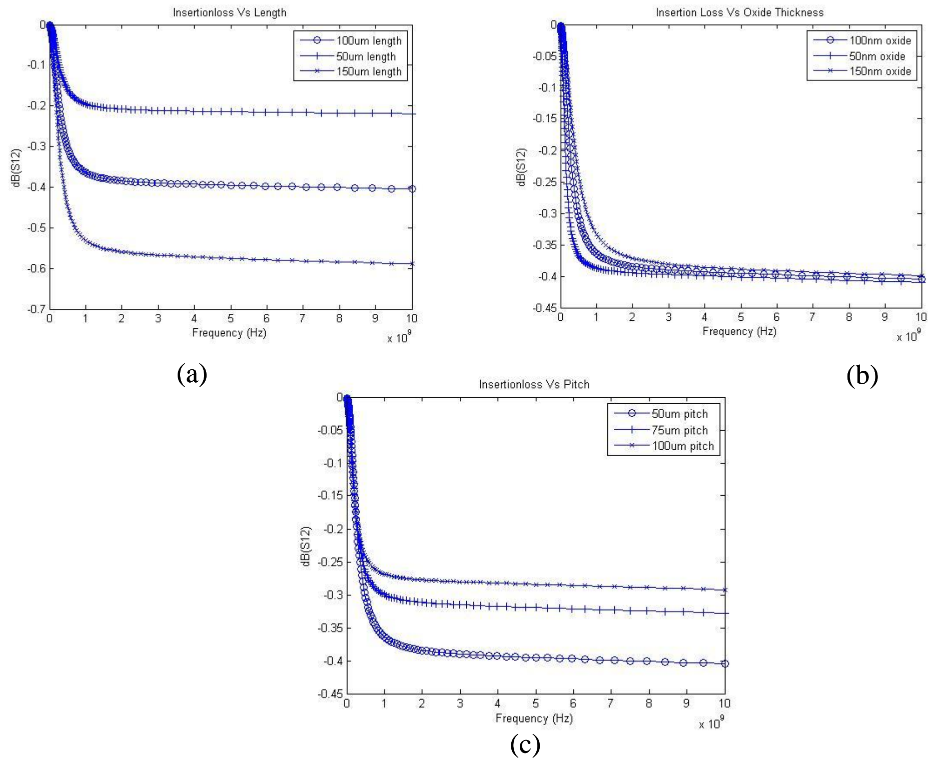


Figure 15: (a) R=10um, dox=0.1um, D=50um; (b) R=10um, L=100um, D= 50um and (c) R=10um, dox=0.1um, L=100um

4. B. Cross Talk and RC Effect

An important effect that needs special attention is the coupling between TSVs. In this section, the coupling between TSV pairs is compared to measurements in the time domain showing the importance of the TSV effect as compared to vias in the inter layer dielectric (ILD) layers. This is followed by a comparison between low and high resistivity silicon substrate.

The structure of the TSV pair is shown in Figure 16 consisting of two TSVs (TSV 1 and 2) with their adjacent ground vias (ground TSV1 and TSV2) [Cho et al, 2011]. The two ground vias are tied together using a ground strap. The cross section consists of the silicon substrate containing the TSV with the ILD on top. The dimensions of the structure are shown in Figure 16 (a). Since this is a two layer structure (silicon substrate and ILD), each layer was modeled separately. The four TSVs were modeled using the cylindrical

basis functions described earlier combined with the modeling of the planar structures such as via pads and ground straps using the PEEC based method [Han, 2009]. All of the coupling between structures in a layer was included in the modeling. For each layer the S-parameters were computed and converted to a spice netlist using Idem [Idemworks, 2009]. The corresponding ports were tied together in Spice to enable continuity of voltages and currents. As described in [Cho et al, 2011], a TDR source was used to excite the structure at Port 1 and the coupled waveform was measured at Port 2. A 50ps TDR pulse source with 2V amplitude was used with 50Ω source and load termination, which included the loss due to the cables. The resulting coupled waveforms (measured and modeled) for pulse periods of 1ns (1GHz) and 10ns (100MHz) are shown in Figure 16 (b) and (c), respectively. The model agrees well with measurements. The modeling results with and without the ILD layer is shown in the figure showing little difference between the two, indicating that the TSV coupling is the dominant mechanism.

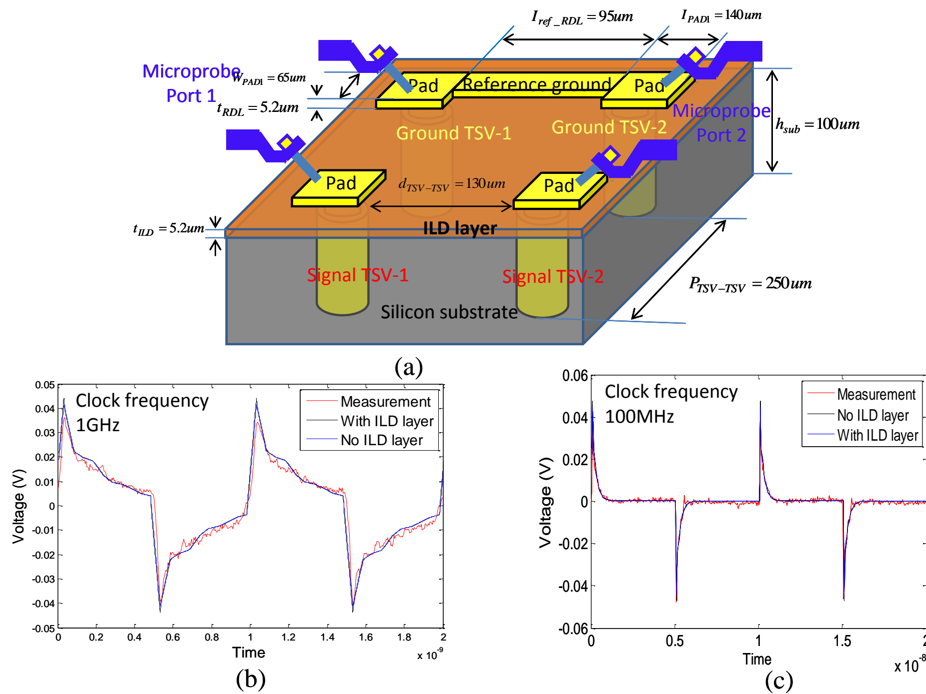


Figure 16: (a) Test Vehicle, (b) Model to hardware correlation for 1GHz clo ck and (c) Model to hardware correlation for 100MHz clock

The cross talk waveform in Figure 16 exhibits a distinct RC behavior leading to a slow decay of the coupled waveform, which is unique to TSVs. This RC effect can be quite detrimental since it can create inter symbol interference (ISI).

As an example consider two TSVs with D=100µm, R=10µm, L=200µm, d_{ox}=0.1µm, ε_{SiO2}=3.9 and ε_{Si} = 11.9 in an array, as shown in Figure 17 (a). Consider two silicon substrates, one with conductivity of 10S/m (low resistivity) and the other with conductivity of 0.01S/m (high resistivity). A pulse with risetime of 100ps and amplitude 2V is propagated through TSV1 using a 50Ω source resistor. The far end of TSV1 and

both sides of TSV2 are terminated in 50Ω. The cross talk waveform on TSV2 is plotted in Figure 17 (b). As can be seen, the 10S/m conductivity silicon substrate leads to 5X larger peak voltage as compared to the 0.01S/m conductivity silicon substrate. Moreover, the low resistivity substrate results in a waveform that has 8X longer coupled noise duration, which can be a significant problem. This difference can be explained by looking at the coupled s-parameters (not shown), where the oxide thickness plays a large role in increasing coupling in the transition region of the TSV. A larger oxide thickness would therefore help in reducing cross talk for low resistivity substrates. In Figure 17, the high resisitivity substrate acts as a low loss dielectric, which is desired. The reason for the excessive coupling is because the silicon substrate is not grounded.

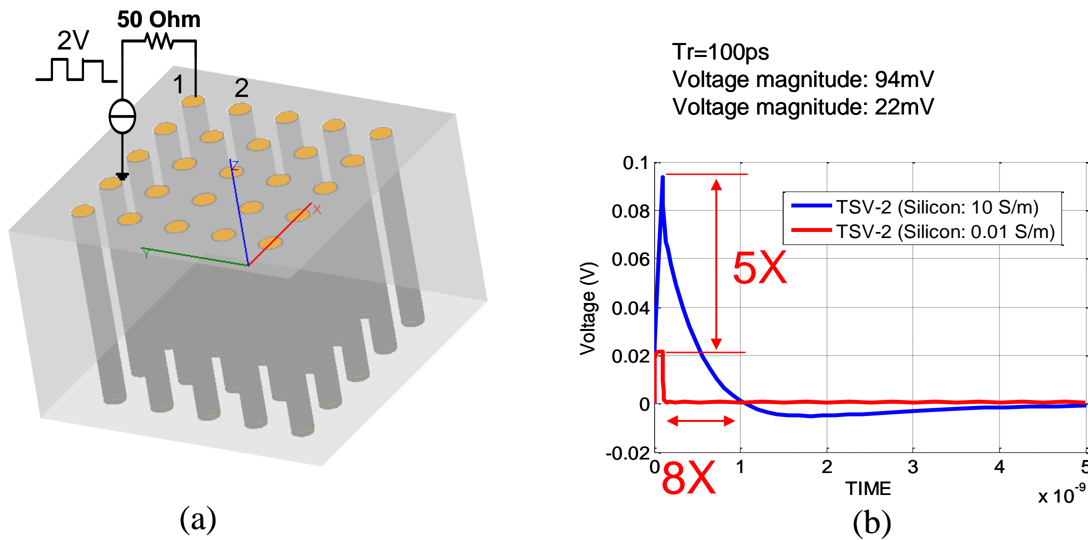


Figure 17: (a) TSV Array with excitation on TSV 1 and cross talk waveform on TSV 2 an d (b) Cross talk waveform for high and low resistivity silicon substrate

4. C. Silicon or Glass Interposer

Interposers used to package stacked ICs contain interconnections, planes and vias (TSV or TGV). When the interconnections are either charged or discharged return currents will always follow the path of least impedance. Any interruption of the return current due to change in reference planes can cause return-path-discontinuities (RPDs). This results in jitter and noise on the signal, proportional to the PDN impedance at the RPD [Swaminathan et al, 2010]. In this section the impact of the vias in conjunction with the interconnections is considered for a microstrip to microstrip transition. Coupling between vias is not considered. An example of a microstrip-to-microstrip transition modeled in CST is shown in Figure 18 (a) and (b) with dimensions. The electrical properties of Si are ε_r = 11.9 and 10S/m conductivity, glass are ε_r = 6.7 and loss tangent of 0.006, and polymer are ε_r = 2.51 and loss tangent of 0.004. A 1 µm thick sidewall liner made of the same polymer is used for the through-via. The microstrip-to-microstrip transition causes a change in the reference plane, creating an RPD. At power plane resonant frequencies, as the PDN impedance increases, this can result in a large simultaneous-switching-noise

(SSN) voltage being induced between the planes. This manifests itself as an increase in the insertion loss of the signal [Sridharan et al, 2011]. Figure 18 (c) shows the insertion loss (S21) for silicon and glass, assuming silicon is replaced with glass, without changing other layers on the stackup shown in Figure 18 (a) and (b). The sharp notches in the insertion loss plot coincide with the power plane resonant frequencies. In the silicon interposer, since the power plane resonances are suppressed, the result is a smooth insertion loss plot, as shown in Figure 18 (c). Though the silicon interposer has higher overall insertion loss, it can lead to a better eye diagram, as discussed in this section.

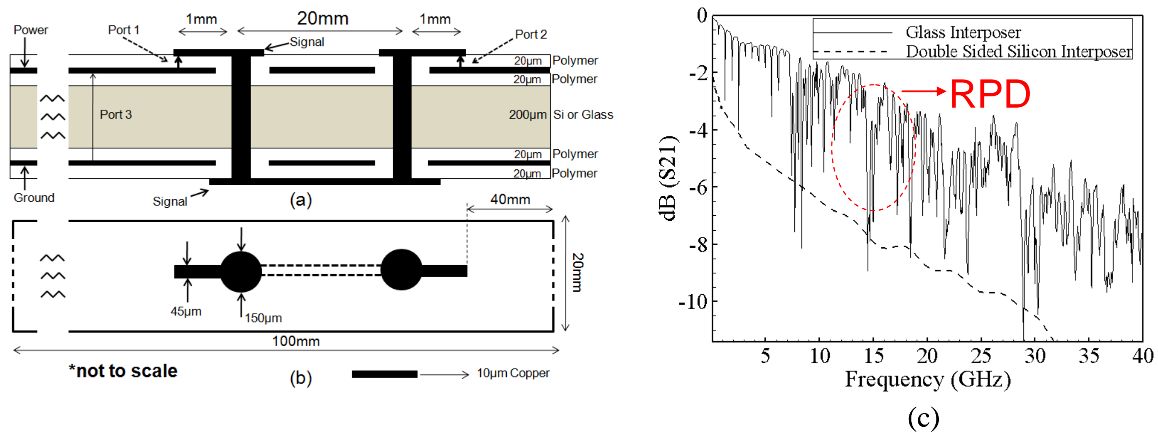


Figure 18: (a) Cross section, (b) Top view of via transition and (c) Comparison of insertio n loss on glass and silicon interposer [Sridharan et al, 2011]

Let's next consider the frequency spectrum of an input bit stream propagating through the interconnection with insertion loss as shown in Figure 18 (c). The frequency spectrum of a pseudorandom bit stream (PRBS) consists of harmonics distributed across multiple frequencies based on the data pattern, as opposed to a simple clock signal. Since the harmonics across multiple frequencies can experience varying insertion losses for glass as shown in Figure 18 (c), it can result in uncertainties in signal amplitudes and also uncertainties in rise/fall times, leading to excessive jitter and reduced eye opening. Figure 19 shows the eye diagram comparison obtained in ADS [ADS, 2009], between glass and silicon interposer for a 3.2 Gbps 2^{10}-1 PBRS stream transmitted between port 1 and port 2 shown in Figure 18 (a). It can be seen that jitter and eye opening are considerably improved in the silicon interposer, in comparison to glass interposer. Depending on the application, however, jitter and eye opening in glass interposer can be improved by suitably adding decoupling capacitors [Swaminathan et al, 2010].

Therefore, though glass has lower loss, variability in the interconnection response can cause excessive jitter and reduced eye height as compared to silicon, since RPDs can dominate the behavior. However, it is important to note that through glass vias (TGV) have much better insertion loss and reduced coupling than TSV (not shown here). Therefore, depending on the manner in which the TSVs, TGVs, interconnections and planes are used to package the stacked ICs, the electrical benefits may not be straightforward.

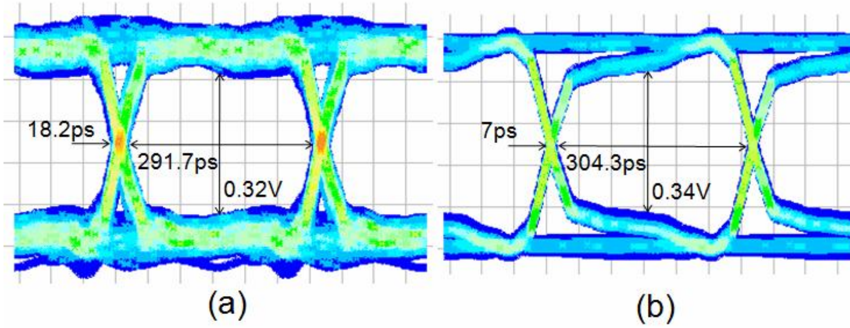


Figure 19: Simulated eye diagrams at 3.2 Gbps for (a) Glass Interp oser and (b) Silicon Interposer [Sridharan et al, 2011]

5. Thermal Modeling and Temperature Effects

Thermal effects play a very important role in dictating both the IR drop and high frequency response of interposers [Xie et al, 2011]. This effect is exacerbated in 3D integration due to larger current densities that need to be supported, resulting in the creation of hot spots in various parts of the system. Joule heating due to current flowing in interconnections can cause increased IR drop while high frequency effects such as cross talk can actually decrease due to temperature increase. These effects are briefly described in this section.

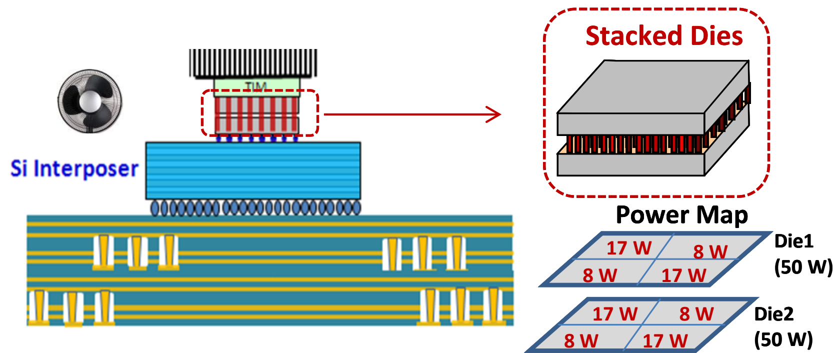


Figure 20: 3D System with Silicon Interposer

Consider a 3D system as shown in Figure 20 consisting of two stacked ICs of size 1.2cm x 1.2cm packaged using a silicon interposer of size 3cm x 3cm mounted on a PCB of size 10cm x 10cm. The IC and interposer thicknesses are 200µm and 110µm, respectively. Thermal interface Material (TIM) of thermal conductivity 2W/m-K is used between the stacked and heat sink to improve thermal conductivity. An ideal heat sink with ambient temperature of 25C is used with air convection coefficient of 20W/m^2-K. The resulting temperature gradient and IR drop (due to Joule heating) in the interposer are shown in Figure 21, where the PCB is powered from the edge (not shown). The temperature gradient in the interposer is between 90C to 104C due to the heat spreading behavior of silicon. The resulting IR drop in the interposer is ~1mV which is quite small (most of the

IR drop is in the PCB due to the larger size). The maximum chip temperature is around 110C which is acceptable for logic die (for memory this temperature is around 85C).

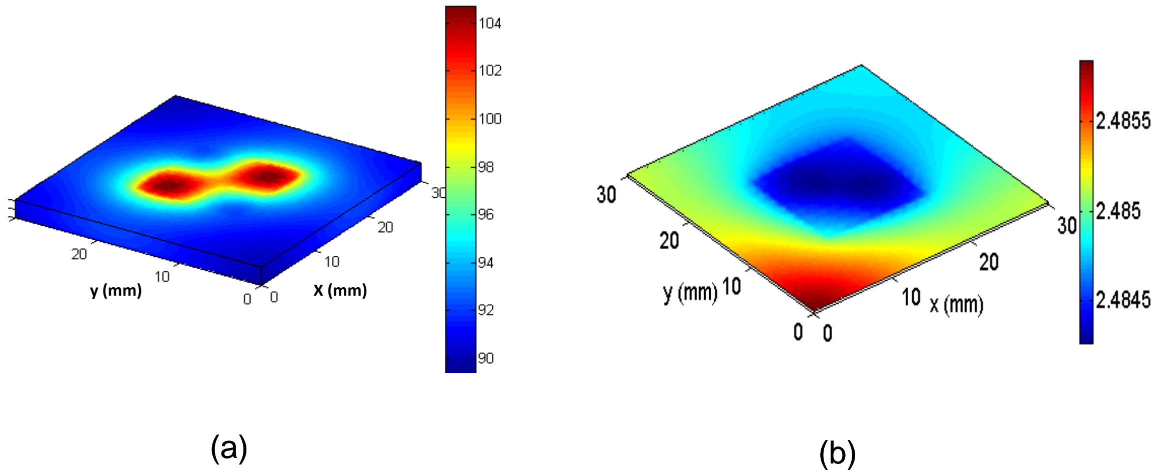


Figure 21: Silicon Interposer (a) Temperature Gradient and (b) IR drop

Another very important effect is the variation of cross talk with temperature. As mentioned earlier, the resistance of TSVs is affected by the conductivity of copper while its conductance is affected by the silicon conductivity.

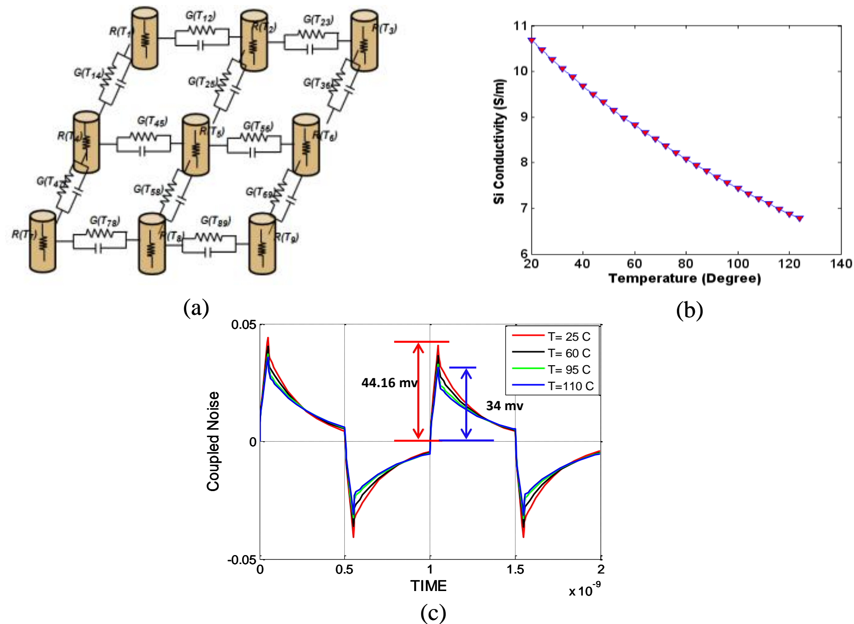


Figure 22: (a) R and G variation with temperature, (b) Silicon cond uctivity variation with temperature and (c) Cross talk waveform var iation with temperature

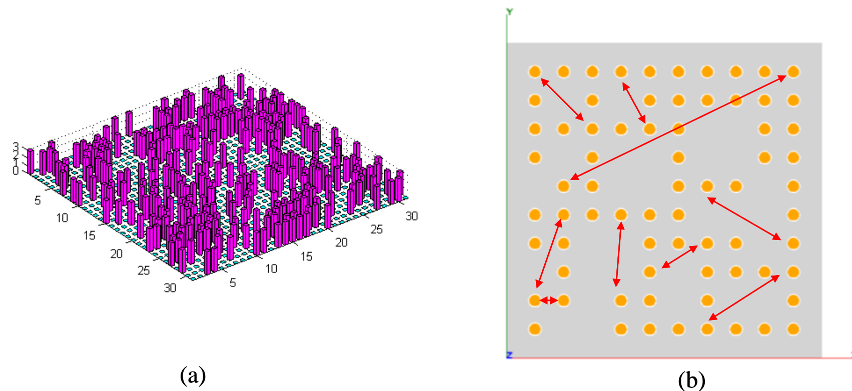
Both the copper and silicon conductivity change with temperature with the silicon conductivity variation having a larger effect on the electrical response (Figure 22 (b)). This is shown in Figure 22 (a) where the resistance R and conductance G become temperature dependent based on the variation of the copper and silicon conductivity with temperature. The cross talk waveform for varying temperatures is plotted in Figure 22 (c) where the peak noise voltage change can be ~25% in the temperature range between 25C and 110C. Clearly, from Figure 22, accounting for temperature effects is essential for estimating the cross talk waveforms.

6. Electrical Modeling Challenges

It appears that the semiconductor and system companies are relying on the silicon interposer solution due to cost reasons. However, the packaging industry seems to be considering the glass interposer due to better properties and potential cost benefits due to larger size panels used for processing. Clearly, both solutions are viable depending on the application. Irrespective of the interposer solution, four major issues need to be tackled from an electrical standpoint namely,

a) Need for handling multi-scale dimensions since the geometries of the structures used can have a scale ratio of 1:1000 or more. Example is the TSV length of 100um with an oxide thickness of 0.1um.

b) Scalability is a very important issue that needs to be addressed. As an example, a silicon interposer not properly grounded can lead to coupling between all the vias. With the presence of Keep Out Zones (KOZ), extracting the TSV parasitics can be quite challenging, as illustrated in Figure 23.



(a) (b)

Figure 23: (a) Placement of TSV accounting for KOZ and (b) TSV to TSV interactions

c) Need for chip – package co-design since the TSV response in the chip stack can propagate into the package. Therefore the RC effect described for TSVs earlier can result in long decaying waveforms in the package even if a glass interposer type of solution is used. An example of a structure with dimensions of a chip stack on an interposer is shown in Figure 24.

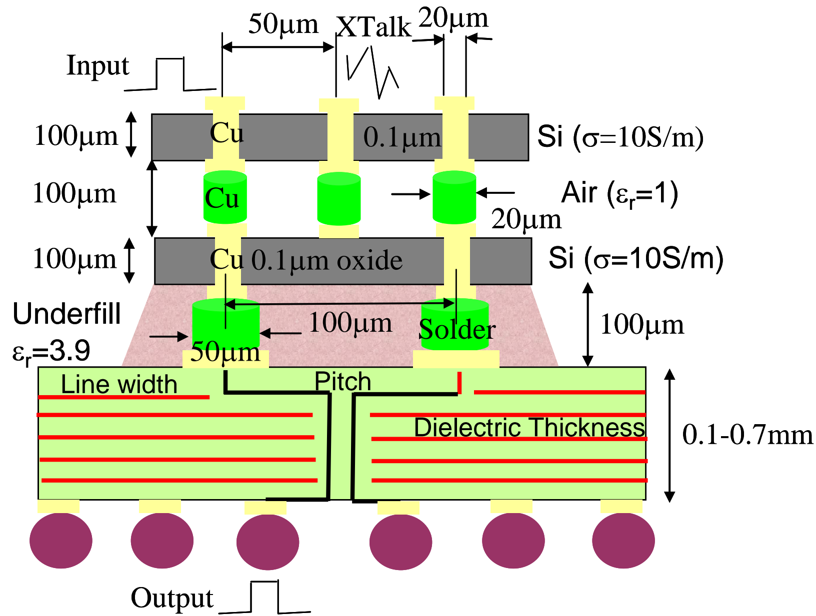


Figure 24: Two stacked chips on a interposer (illustration only) requiri
ng chip-package simulation for analyzing interactions

d) Need for including temperature effects as described earlier to compute the IR drop due to Joule heating and high frequency effects.

The rigorous electromagnetic analysis method described earlier for analyzing TSV arrays has the capability of handling large numbers of TSVs simultaneously as illustrated in Figure 25. It also has the capability of addressing the multi-scale dimensions involved. This has been combined with models for short planar interconnect structures using the PEEC method and is also being coupled to the Multi-layered Finite Difference Method [Swaminathan et al, 2007] at Georgia Tech. They also form the framework for the Sphinx suite of tools [Sphinx 3D Path Finder and Sphinx, 2011].

7. Standardization

To facilitate a smooth transition from today's 2D design flows to next-generation flows for 3D ICs and interposers, it is essential to proactively develop standards for 3D IC design in a timely way. This requires Design Exchange Formats (DEF) and point tool development in two major areas initially namely, thermal and power delivery analysis. These have been identified by Sematech/SRC/Si2 working together with semiconductor companies. Several universities such as NCSU, UCSD, UMN, UCLA and Georgia Tech are involved in this initiative. A first draft of the requirements has been submitted to Sematech/SRC based on a collaborative effort from the universities mentioned above.

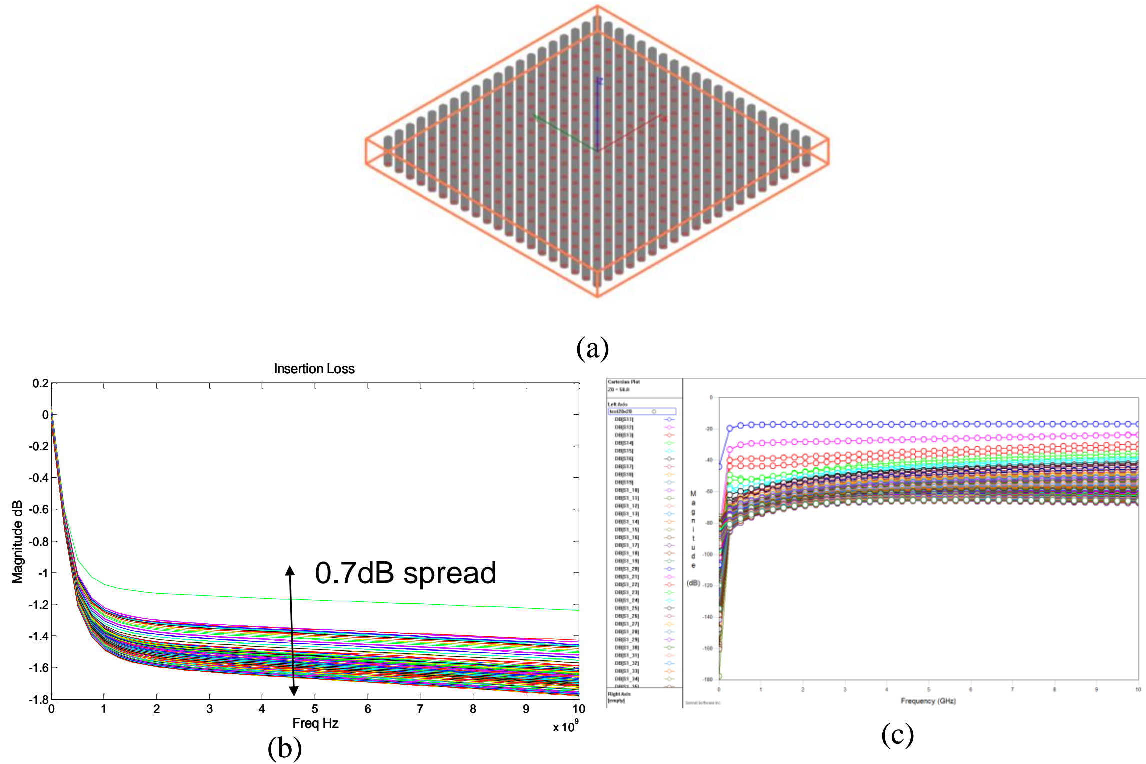


Figure 25: (a) 20 x 20 TSV Array, (b) Insertion Loss of 400 TSVs showing 0.7dB spread and (c) Near End Cross Talk (R=10µm, L=100µm, D=50µm, Silicon conductivity = 10S/m, copper conductor, er of SiO2 = 3.9, er of Si = 11.9

8. Summary and Conclusions

It is clear that 3D integration will be the next big wave in the semiconductor industry for continuing Moore's law. This enables reduction in package footprint but the main driver is a reduction in power and increase in bandwidth, especially for logic to memory communication (mobile) and logic to logic communication (FPGA). Today, the mobile and FPGA applications benefit the most with 3D integration.

Interposers play a very important role in 3D integration from an electrical, thermal and mechanical stand point. Electrical modeling of these interposers is not trivial especially for silicon substrates due to its lossy and semi-conducting behavior along with the multi-scale dimensions involved. In addition, temperature effects are very important as well.

In this paper, the electrical challenges and potential solutions for the modeling and design of interposers (mainly silicon and to a lesser extent glass) have been discussed.

9. Acknowledgement

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