Fifth IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits

3D-TEST

in conjunction with ITC / Test Week 2014
Washington State Convention Center – Seattle, WA, USA
October 23+24, 2014
http://3dtest.tttc-events.org

Call for Submissions

The 3D-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional stacked ICs (3D-SICs), including Systems-in-Package (SiP), Package-on-Package (PoP), and especially 3D-SICs based on Through-Silicon Vias (TSVs), micro-bumps, and/or interposers. While 3D-SICs offer many attractive advantages with respect to heterogeneous integration, smaller form-factor, higher bandwidth and performance, and lower power dissipation, there are many open issues with respect to testing such products. The 3D-TEST Workshop offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

3D-TEST will take place in conjunction with the IEEE International Test Conference (ITC) and is sponsored by the Test Technology Technical Council (TTTC) of IEEE Computer Society.

Topic Areas – You are invited to participate and submit your contributions to the 3D-TEST Workshop. The workshop's areas of interest include (but are not limited to) the following topics:

- *Defects due to Wafer Thinning*
- *Defects in Intra-Stack Interconnects*
- *DfT Architectures for 3D-SICs*
- *EDA Design-to-Test Flow for 3D-SICs*
- *Failure Analysis for 3D-SICs*
- *Fault-Tolerant Design for 3D-SICs*
- *Interposer Testing*
- *Known-Good Die / Stack Testing*
- *Power and Heat Dissipation during Test*
- *Pre-Bond, Mid-Bond and Post-Bond Test*
- *Reliability of 3D-SICs*
- *Stacking Yield of Dies and Interconnects*
- *Standardization for 3D Testing*
- *System/Board Test Issues for 3D-SICs*
- *Test Cost Modeling for 3D-SICs*
- *Test Flow Optimization for 3D-SICs*
- *Tester Architecture incl. ATE and BIST*
- *Thermal/Mechanical Stress in 3D-SICs*
- *TSV Test, Redundancy, and Repair*
- *Wafer Probing and Probe Marks of 3D-SICs*

Submission Instructions – Submissions must be sent in as PDF file. The Workshop prefers Full Paper submissions (of up to six pages), but also allows Extended Abstract submissions (of at least two pages). Detailed submission instructions can be found at the Workshop's website: http://3dtest.tttc-events.org. All submissions will be evaluated for selection with respect to their suitability for the workshop, originality, technical soundness, and presented results. Selected submissions can be accepted for regular or poster presentation at the Workshop.

Publications – The workshop will make available to all participants an Electronic Workshop Digest, which includes all material that authors are willing to provide: abstract, paper, slides, poster, etc.

Key Dates

- Submission deadline : **September 8, 2014**
- Notification of acceptance : **September 22, 2014**
- Camera-ready material : **October 6, 2014**

Further Information

Yervant Zorian – *General Chair*
Synopsys
700 East Middlefield Road
Mountain View, CA 94043-4033, USA
Tel.: +1 (650) 584-7120
E-mail: yervant.zorian@synopsys.com

Erik Jan Marinissen – *Program Chair*
IMEC
Kapeldreef 75
B-3001 Leuven, Belgium
Tel.: +32 (0)16 28-8755
E-mail: erik.jan.marinissen@imec.be