Fifth IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits

3D-TEST

in conjunction with ITC / Test Week 2014
Hyatt Hotel at Olive 8 – Seattle, WA, USA
October 23+24, 2014
http://3dtest.tttc-events.org

Call for Participation

The 3D-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional stacked ICs (3D-SICs), including Systems-in-Package (SiP), Package-on-Package (PoP), and especially 3D-SICs based on Through-Silicon Vias (TSVs), micro-bumps, and/or interposers. While 3D-SICs offer many attractive advantages with respect to heterogeneous integration, smaller form-factor, higher bandwidth and performance, and lower power dissipation, there are many open issues with respect to testing such products. The 3D-TEST Workshop offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

3D-TEST will take place in conjunction with the IEEE International Test Conference (ITC) and is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society.

Workshop Program – The workshop program contains the following elements.

- Keynote Address: "3D Rock from the Sun" by Brion Keller, Senior Architect Encounter Test at Cadence Design System.
- Invited Address "What a Difference a Year Makes – Looking Back and Forward" by Herb Reiter, President of eda2asic Consulting.
- Two sessions with in total seven paper presentations.
- Two panel-discussion sessions
  - On "3D Memories: What Is Coming And How Are We Going To Test That?"
  - On "2.5D-SICs: Do We Need To Test The Interposer, And If So, How?"
- A special session on the status of IEEE P1838 test access standard.
- A special session on ongoing PhD research in 3D-Test.
- Continuous display of table-top demos and posters.

For the detailed version of the program, please turn over.

Participation – You are invited to participate in the workshop. Participation requires registration and a registration fee. Workshop registration includes access to all technical sessions, Electronic Workshop Digest (containing extended abstracts, papers, slides, posters, as made available by their presenters), workshop reception, continental breakfast, lunch, and break refreshments. On-line registration is available via the workshop's website (http://3dtest.tttc-events.org). Alternatively, register on-site during Test Week at the ITC Registration Counter at the Washington State Convention Center; admission for on-site registrants is subject to availability.

Further Information

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Workshop Program

Thursday October 23, 2014

Session 1: Opening

Moderator: Eric Hill – Cascade Microtech, USA

17:00h: **Welcome Address**
General Chair: Yervant Zorian – Synopsys, USA
Program Chair: Erik Jan Marinissen – IMEC, Belgium

17:10h: **Award Ceremonies**
- Presentation of 3D-TEST 2013 Best Paper Award:
  In-Place Signal and Power Noise Waveform Capturing Within 3D Chip Stacking
  Makoto Nagata, Satoshi Takaya – Kobe University, Japan
  Hiroaki Ikeda – ASET, Japan
- IEEE Service Awards

17:15h: **Keynote Address**
3D Rock from the Sun
Brion Keller – Sr. Architect Encounter Test -- Cadence Design Systems, USA

A quick look at future products that may pull us into the 3rd dimension.

Session 2: Special Session

18:00h: **IEEE P1838: What Is It and What Is It Not?**

Moderator: Marc Hutner – Teradyne, Canada

Speakers: Erik Jan Marinissen – Principal Scientist – IMEC, Belgium
Adam Cron – Principal Engineer – Synopsys, USA
Teresa McLaurin – DfT Technical Lead/Manager – ARM, USA
Sandeep Bhatia – Tech Lead Manager – Google, USA

IEEE P1838 is defining a standardized 3D-DfT architecture for (scan) testing of 3D-SICs. Last year, the Working Group formed three sub-teams ("Tiger Teams") on (1) Serial Control, (2) Die Wrapper Register, and (3) Flexible Parallel Port, and has made significant progress since then. In this Special Session, four active members of the P1838 Working Group will present an update on the current status of the standardization effort.

Workshop Reception

19:00-21:00h

Friday October 24, 2014

Workshop Breakfast

07:00-08:00h

Session 3: Special Session

08:00h: **Ongoing PhD Research in 3D-Test**

Moderator: Bill Eklow – Cisco Systems, USA

08:00h: Test and Debug Solutions for 3D-Stacked Integrated Circuits
Sergej Deutsch, Krishnendu Chakrabarty – Duke University, USA
08:15h: Redundancy Architectures and Analysis Methodologies for 3D Memories Yield Improvement
Bing-Yang Lin, Cheng-Wen Wu – NTHU, Taiwan
08:30h: Pre-bond TSV Test Optimization and Stacking Yield Improvement for 3D ICs
Bei Zhang, Vishwani Agrawal – Auburn University, USA
08:45h: Panel Discussion

Session 4: Papers

Moderator: Martin Keim – Mentor Graphics, USA

09:00h: Cross-Die BISR Design for the 3D-Stacked Wide-I/O DRAM
Ming-Hsueh Wu, Kun-Lun Luo, Chun-Lung Hsu, Bing-Chuan Bai – ITRI, Taiwan
09:20h: Power-Supply-Noise-Aware Dynamic Timing Analyzer for 3D IC
Hung-Yi Hsieh, Cheng-Yu Han, and James Chien-Mo Li - National Taiwan University, Taiwan
09:40h: Delay Line Embedded in Boundary Scan for Testing TSVs
Hiroyuki Yotsuyanagi, Hiroki Sakurai, Masaki Hashizume – University of Tokushima, Japan

Session 5: Table-Top Demos and Posters

10:00h: For list of Posters and Table-Top Demos: see next page.
Coffee and tea provided.

Session 6: Panel Discussion

10:30h: **3D Memories: What Is Coming And How Are We Going To Test That?**

Moderator: Françoise von Trapp – Queen of 3D – 3DInCites, USA

Panelists: Jonathon E. Colburn – Principal DfT Engineer – nVidia, USA
Gary Fleeman – Industry Expert – USA
Marc Greenberg – Director Product Marketing – Synopsys, USA
Bob Patti – CTO – Tezzaron Semiconductor, USA
Betty Prince – CEO – Memory Strategies Internationa, USA

Memories are among the first semiconductor products to harvest the benefits of 3D stacking technology, with and without through silicon vias (TSVs). This panel will discuss the different 3D memory structures being introduced to the market, including 3D NAND flash and 3D DRAM, how these 3D memories are enabled by 3D technology, what technology benefits will be realized by products integrating 3D memories, which ones will make it to the market, what are the associated test challenges, and how will they be addressed. The panel will kick off with a real-time, on-line audience poll to gauge the audience opinion. The panelists will then address the same questions. Discussion is encouraged.

Workshop Luncheon

12:00-13:00h

Session 7: Papers

Moderator: Ira Feldman – Feldman Engineering, USA

13:00h: CDM ESD Testing of a 3D TSV Stacked IC Chip
Makoto Nagata, Satoshi Takaya, Hiroaki Ikeda – Kobe University, Japan
Dimitri Linten, Mirko Scholz, Shih-Hung Chen – IMEC, Belgium
Keiichi Hasegawa, Taizo Shintani, Masanori Sawada - Hanwa Electronic, Japan
13:20h: Electrical Fault Isolation and Signal Mapping in 3D IC
Jan Gaudestad, Antonio Arozco – Neocera, USA
13:40h: A Low-Cost Method for Wafer Sort Test of Interposer Dies
Amitava Majumdar, Raghunandan Chaware, Ganesh Hariharan – Xilinx, USA
14:00h: TSV Leakage in Si-Interposer and 3D Silicon
TM Mak, Eddy Lo, Raymond Seah – GLOBALFOUNDRIES, USA

Session 8: Invited Talk

Moderator: Erik Jan Marinissen – IMEC, Belgium

14:20h: What a Difference a Year Makes – Looking Back and Forward
Herb Reiter – President – eda2asic Consulting, USA

Most people agree that designing multiple dies into one package, using high-speed interconnects, and testing all, represents a major change for our industry, that clearly needs to improve time-to-market, speed, power, form-factor, and eventually IC cost. The same people tend to complain about the slow progress 2.5D/3D seems to make – at a cursory look. This talk looks back a year, to key successes, and forward, at least a year, to show how packing multiple dies into one IC package will change our lives.

Session 9: Panel Discussion

14:50h: **2.5D-SICs: Do We Need To Test The Interposer, And If So, How?**

Moderator: Jan Vardaman – President – TechSearch International, USA

Panelists: Sandeep K. Goel – Academician/Senior Manager – TSMC, USA
Said Hamdioui – Associate Professor – TU Delft, the Netherlands
Gerard John – Technical Director Test Dvlpmnt – Amkor Technologies, USA
Choon-Leong Lou – CEO – STAr Technologies, Taiwan
Amitava Majumdar – Principal Engineer – Xilinx, USA
TM Mak – Director 2.5D/3D DfT Strategy – GLOBALFOUNDRIES, USA

'2.5D-SICs' is the informal, popular term for semiconductor products consisting of active dies, stacked side-by-side on an interposer substrate. These interposers are typically passive silicon substrates, containing only TSVs and BEOL interconnnect, implemented in a low-cost, mature technology. Do we need to test such interposers in pre-bond, mid-bond, and post-bond stages, or can we simply count on it being defect free? And if we need to test the interposer, how?

Workshop Closure

16:10h

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Posters and Table-Top Demos

Posters

Posters are on display throughout the workshop.
Dedicated poster session

- Friday October 24: 10:00-10:30h

Poster 1: Diagnostic Tests for Pre-Bond TSV Defects
Bei Zhang, Vishwani Agrawal – Auburn University, USA

Table-Top Demos

Table-top demos are on display throughout the workshop.
Dedicated demo session

- Friday October 24: 10:00-10:30h

Demo 1: Process and Test Flow Development for 3D-Integrated Heterogeneous Systems
Armin Grünewald, Michael Wahl, Rainer Brück – University of Siegen, Germany
Demo 2: 3D Test Advances in Substrate and Interposer Testing with the STAr Gemini Hybrid ATE
Choon-Leong Lou – STAr Technologies, Taiwan;
Nick Gullett – Semiconductor Consultants, USA
Demo 3: 3D-IC Implementation and Testing
Adam Cron – Synopsys, USA
Demo 4: Pyramid Probe Card
Ken Smith – Cascade Microtech, USA

Corporate Supporters

The 3D-TEST Workshop gratefully acknowledges the financial support from the following companies

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