Range of applications

More than 1 000 000 pacemakers and more than 200 000 defibrillators are implanted in the world each year. Infusion pumps for diabetes and pain are more than 200 000 devices implanted per year. Neurodevices implanted for pain management, epilepsy, Parkinson and many others are growing rapidly currently more than 150 000 are implanted each year. In 2010, 219 000 people worldwide had cochlear devices implanted. In the U.S alone some 900 000 people are believed to be deaf or near deaf. In India, there are an estimated 1 million profoundly deaf children; only about 5,000 have cochlear implants. All these devices need 3D heterogeneous integration to reduce the size of the electronics. The main indication for pacemaker implantation is the atrioventricular block. In 2012, 4.89 million people are supposed to have this pathology worldwide. Global market revenue for pacemakers in 2012 was $4.3bn

Leadless pacemakers are expected to be revolutionary to the CRM industry, especially in the US and EU by eliminating the need for lead replacement. The state of the art for the volume of a subcutaneous pacemaker is 8 cm^3. The state of the art for the volume of a leadless pacemaker is 1.5 cm^3.

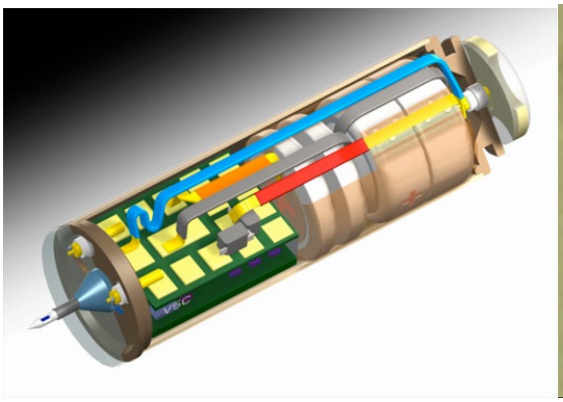

Figure 1 : leadless pacemaker prototype from SORIN

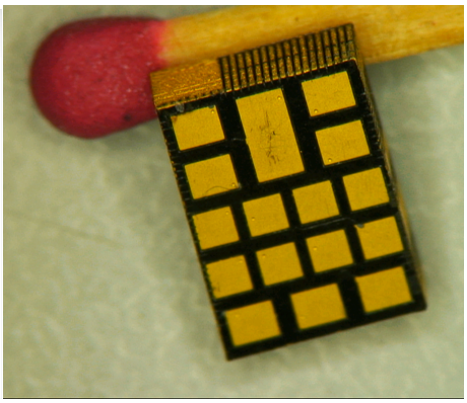

Figure 2: 3D IC heterogeneous integration from 3D+ ($2.3*5.2*7.3mm^3$)

Yield of 3D IC heterogeneous integration

3D IC wafer level stacking raises the issue of yield and consequently cost

If 4 levels of wafers are stacked and if the yield of each level is 95%, the global yield is expected to be 81%. If 4 levels of wafers are stacked and if the yield of each level is 90%, the global yield is expected to be 65%. If 4 levels of wafers are stacked and if the yield of each level is 85%, the global yield is expected to be 52%.

The wafer level stacking could be a nightmare regarding the yield. It was the main **reason in developing the stacking of known good rebuilt wafers.**

A lot of works and papers have been made for more than 10 years, with the stacking of the wafers with the use of Thru Silicon Via (TSV). The TSV are mainly used with the MEMS and imagers, which have the need of a small quantity of TSV per chip (around 10 or less).

Unfortunately, the stacking of wafers with memory, Asic, µprocessor did not work in production for the following reasons:

- The yield (Y1) of the wafer could be from 80 to 95% and the stacking of them leads to a global low yield,
- The yield of each TSV (Y2), generally the redundancy by 3 even by 6 are used in order to increase the yield, but the global yield of this step stays relatively low,
- The yield of the bonding of all the TSV of the wafer level “n” to the wafer level “n - 1” (Y3) has to be considered too,
- The multiplication of Y2, Y3 and “n” times Y1 leads to a very low global yield.

The yield has been addressed for the leadless pacemaker 3D module by extensive electrical tests done for every component used before assembly.

The layers of the 3D modules have been electrically tested before stacking. The yield on each layer, as every single component has been tested, is more related to the manufacturing process. The manufacturing yield for all the layers resulted acceptable for production due to the maturity of the process used either eWLB or PCB.

The thermal resistance between memories for instance stacked on a µprocessor is low, and the temperature of both die is very close, which is bad for the memory; there is no thermal decoupling between them. In order to solve these problems 3D PLUS has launched the stacking of Known Good Rebuilt Wafers, which is a wire free die on, die (WDoD) approach.

The different reconstructed wafers are glued with an automatic wafer stacking equipment, then the dicing of the “n” reconstructed wafers allows to see each cross section of the copper trace inside the RDL of each wafer. The dicing streets of the stacked wafers are plated with electro less deposition, then an automatic laser patterning allows to interconnect the different cross-section from each level. Any kind of die can be used (no need of a specific die with TSV).

With this technology, only known good wafers are stacked, the reconstructed wafers have been made with fan-out technology; the global yield is very high.

3D-integrated systems and electrical parasitics

Nearly all 3D-integrated systems suffer from electrical parasitics, which are originally not taken into account during the 2D-design phase. Therefore it is necessary to perform an extraction of those parasitics and developed an appropriate workflow. As an example, in the E-BRAINS project, FHG-IIS-EAS took the 3D module developed by Sorin and 3D Plus. They extracted parasitic capacitances of different nets in different layers of the stack. The mutual capacitances form a parasitic network, which is added to the original design und thus enables an electrical simulation of the whole system.

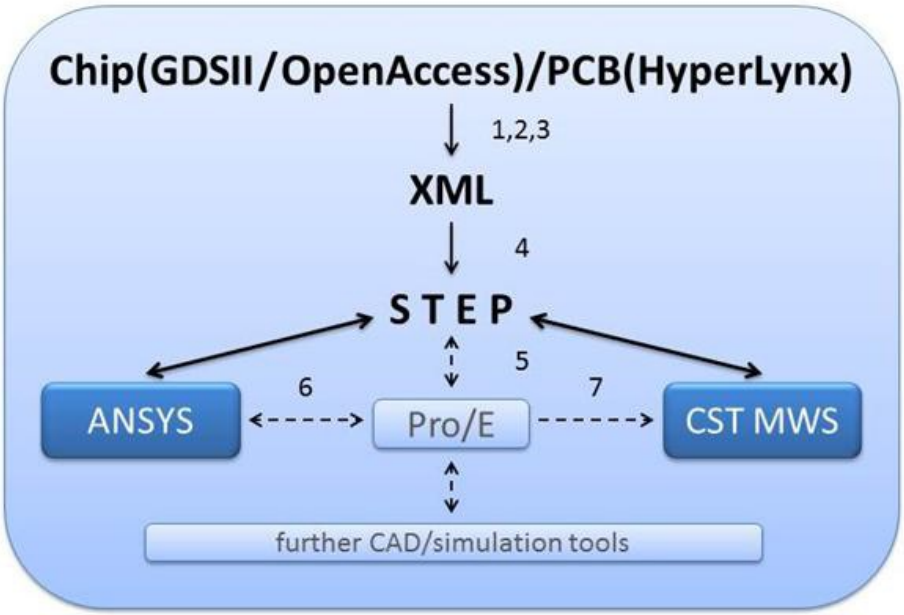

Figure 3 Converting the XML based description to standard FEM tools

Embedded PCB versus 3D IC for a leadless pacemaker prototype

The size of the leadless pacemaker 3D IC heterogeneous module is 2.3*5.2*7.3mm^3. The module has 4 layers stacked using 3D+ WDoD (Wirefree Die on Die) process from 3D Plus. The layers are stacked on wafer level. 2 layers have known good passive (30) and active components (3) and are reconstituted wafers using fan out WLP technology eWLB. RDL pitch is 100µm. The 2 other layers are PCB based. The stacking is performed on Known Good Rebuilt Wafer KGRW. The comparison between Embedded IC in the PCB versus WDoD allows to show the main differences between these two technologies. The Embedded IC in the PCB presents some distinctive characteristics:

- -The small die are used,
- -The moving of the die during the curing of the PCB is more important than with the Fan-out technology,
- -If several dice are embedded, the accuracy of their location could be critical (one of the advantage of the Fan-out is the use of an isotropic epoxy resin with silica filler),
- -A full system with different die and passive components will have a large area due to the fact that it is 2D technique.

.

Conclusion

Manufacturing of 3D IC heterogeneous integrated modules for all the electronics of a leadless pacemaker in a very small volume has been realized and feasibility has been proven. Manufacturing of 3D IC modules using the described process is ready for medium volume production.