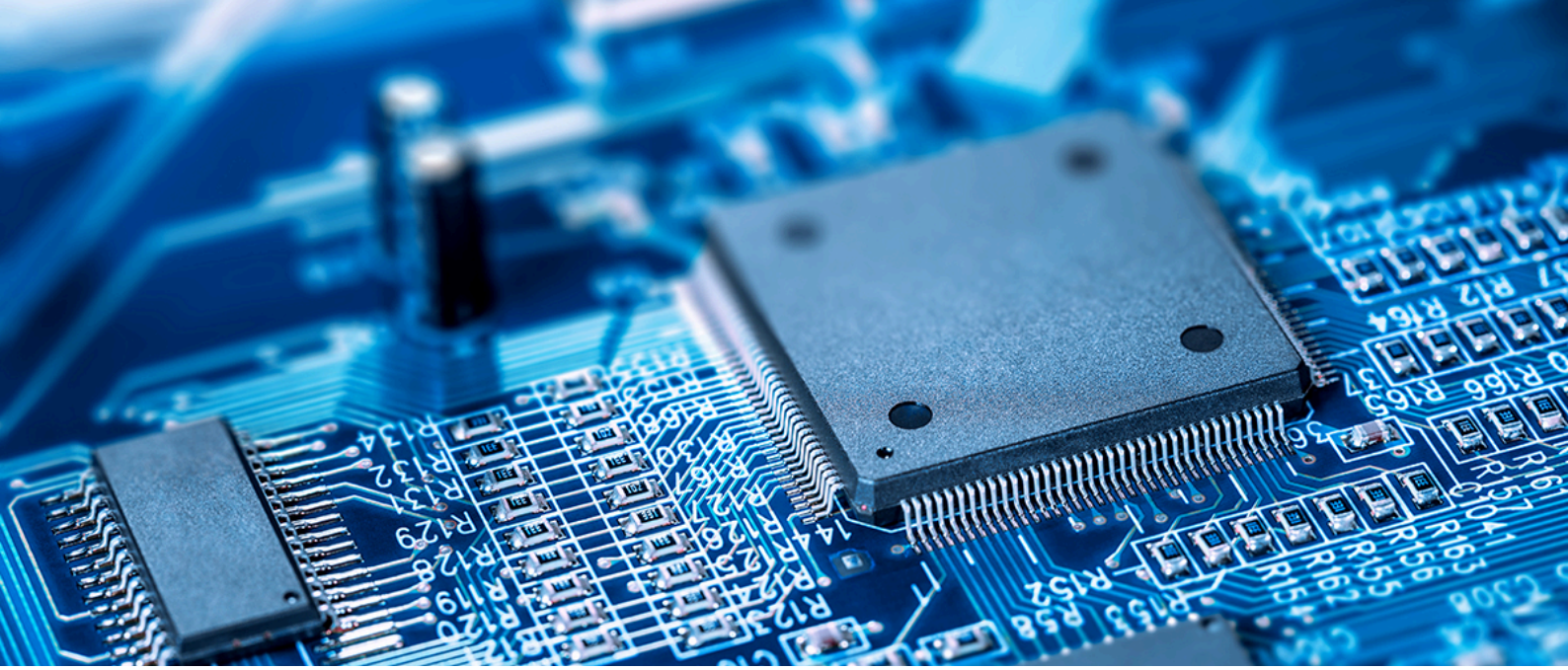

DIGITAL INDUSTRIES SOFTWARE

An organic package designer's guide to transitioning to FOWLP and 2.5D design

Executive summary

The IC packaging design tool set has matured to the point where it can address not only classic plastic, organic and ceramic packaging substrates but can also address silicon substrates driven by interposer and chiplet designs. In most cases system and packaging teams do not have to abandon their existing tool set to support these designs. In fact, the packaging design tool set can offer additional capabilities with respect to multi-component system design and component stacking better than an IC layout tool.

This paper shares insights based on the experiences of organic package substrate designers who have transitioned and mastered RDL-based FOWLP and 2.5D silicon and organic interposer design, while still using (and preserving) the majority of their existing packaged design tools and skills.

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Introduction

Many package designers have many years of hands-on experience designing organic FR4/HDI build-up BGA/LGA substrates. We've memorized the design guidelines and the substrate fabrication is well understood. We know how to wield our design tools like precision scalpels to get the design completed on-time, on-specification and on budget. Whether it's flipchip attach, wire bond or a stacked die combo the design methodology is well understood.

Then management mentions that the next generation of designs are going to be heterogeneously integrated, utilizing new integration platforms such as RDL-based fan-out wafer level and/or interposers. Suddenly, people start mentioning things like assembly design kits, stream-out, sign-off using PDK's, multi-pass degassing, seal rings, assembly LVS and HBM stack routing. The suggestion is made that new design tools might be needed – semiconductor place-and-route tools that only work on Linux and are all TCL/TK script driven. We start doing some research online and attend a conference or two and listen to some of the EDA tool vendors and you could easily arrive at a point where you start to think: Am I obsolete? Do I really need to learn to use silicon place-and-route tools? What is assembly LVS? What is multiple pass degassing? And why do my metal planes need to be hatched and offset?

For many of us, the shift in technology can be overwhelming. Do not despair; yes, there is new terminology to understand and many new design techniques to be understood and mastered, as well as a completely new design process and flow. The good news is that this can all be overcome without having to learn silicon place-and-route design tools.

We have clearly entered a domain of design where once there was a clear-cut delineation between silicon die design and IC packaging design, and now there is an overlapping design domain where silicon foundries are generating substrates and OSATs are using silicon as substrate material; the lines between these two design domains have blurred. Can the IC packaging design tools be used to design silicon substrates?

System approach

Silicon interposers, 2.5D integration, and 3D stacking serve as a bridge between the higher I/O density of today's large die and the PCB, or a system-level substrate. Is a silicon substrate design an IC design challenge or an IC packaging design challenge? This is not a new question, and we've been considering these design domain questions for at least 10 years. As an IC package designer, we don't have to abandon our packaging tools and learn IC place-and-route design tools to generate a silicon substrate design. In most cases, the IC packaging tools are more than adequate to design a silicon substrate, using a silicon PDK, and in many aspects may be the preferred tool. We'll talk about this more later.

Silicon substrates (e.g., interposers, chiplet-based designs) are a disruptive technology. They fall squarely in-between classic implementation of IC design and package design. “Course” interposers (those with line-space rules greater than five microns) can easily leverage IC packaging tools to accomplish their design task. But even for “fine” interposer technology (those that are one micron line-space, or even smaller) the IC packaging tools can still provide a viable, if not preferred toolset to accomplish this task. The IC packaging designer need not abandon their current tools; the design rules are very IC-like and the manufacturing checks will also be IC-based. But except for some very specific areas, the IC packaging layout tools can support these silicon substrates.

IC technology-based solutions follow classic IC design and are focused on IC design problems e.g., timing analysis, manufacturing-ready DRC, layer-based biased routing and placement organization. They are almost always focused on and optimized for a single die design. Packaging and PCB technology-based solutions focus on multi-component, system interconnect analysis and organization. PCB and packaging design technology takes a system-level approach, optimized for multiple dies, substrates, and discrete components.

Likewise, the determination of who within an organization performs a silicon-based interposer or substrate design can be driven by historical and external forces. What silicon process node is being used for the silicon substrate? What IC design structures are required at this process node, including things like power striping and redundant vias? What materials are used for the metals and the dielectrics within the design? Who will ultimately manufacture the silicon? Is it a foundry, or will you be using an OSAT, adding additional metal layers to a design? What is required for IC implementation and mask generation?

The digital IC silicon layout tools tend to focus on a single die, and clearly, with the disaggregation of large SOCs, the advent of chiplet technology, systems with a large processor and multiple stacks of memory may not be a good match for a single-die-centric tool. A tool, such as Xpedition Substrate Integrator (xSI), that can plan, manage, and analyze an entire system early in the design process is clearly advantageous. There is clearly a need to organize and optimize an entire system early in the process and provide the ability to perform preliminary analyses to avoid late, expensive changes in the design. (Figure 1). A system planning and organization tool, like xSI, that feeds into an instance of the implementation tool, e.g., Xpedition Package Designer (xPD), for each of the die and substrates in the design and a tool (like Calibre3DSTACK) that can provide the system verification and confirmation at the end of the process are both highly desirable; all these tools exist in the IC packaging design domain.

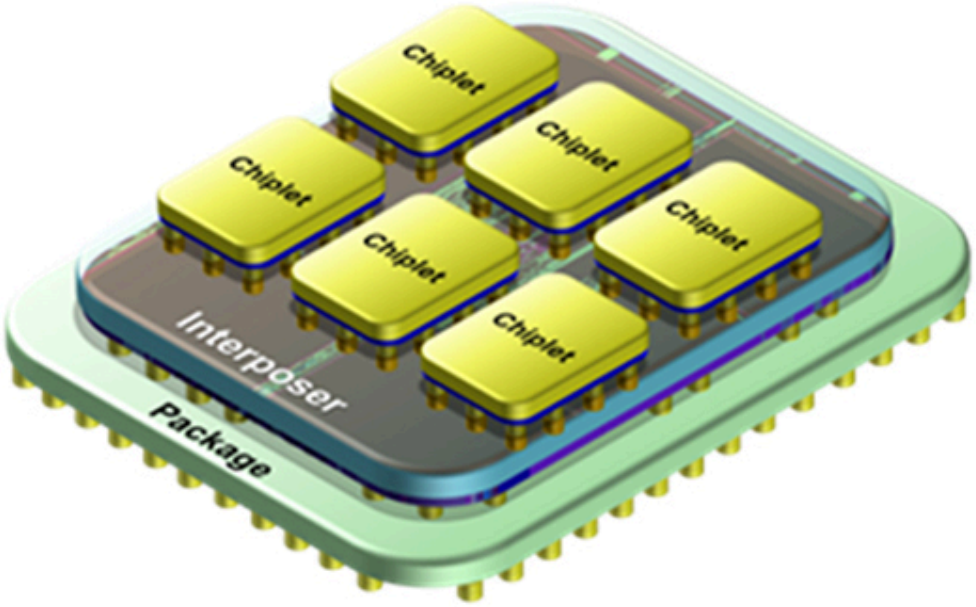

Figure 1. It's a system (image provided by CEA-Leti).

Co-design

Within the system being designed there may be opportunities to organize, and possibly modify, the connections between the different components, optimizing for layout (routing, layer count) as well as performance (SI, PI, Thermal). If the die components are not off-the-shelf and are in the process of being designed while the overall system is being designed, the system tool can leverage "co-design" between the die and the interposer or packaging domains to optimize chip I/O pad ring placement, substrate placement, and stacking organization. This will provide the shortest and best signal and power response as well as minimize the number of layers and the obstruction and congestion challenges when routing the design. Die pad rings can be laid out within the context of the interposer or the substrate to optimize routing and minimize the number of layers in the design, which of course reduces cost.

The designer can look at the design in the 2D (placement, orientation) and 3D (stacking) spaces, evaluating the density and placement of the bumps within the design to ensure there is sufficient power going through the design, and optimize the interconnect between the elements of the design. They can manage the nets across multiple domains (often with different names in each domain). They can examine and assign system connections, looking at the connection points for the various die, substrates, and discrete components and optimize the placement and organization of the design to minimize routing crossovers, provide sufficient power delivery and put the design into the smallest form factor (Figure 2).

The designer can also look at the interconnect and perform feasibility studies and assess different configurations (stacking and placement). There may also be opportunities early in the design process to define the grouping and partitioning of the design.

The ability to bring the system into a single planning tool, like xSI, can allow system level SI/PI/Thermal analysis and co-simulation across multiple fabrics

and multiple layers accounting for the internal routing as well as the component interconnect.

IC packaging has come into its own, where once traditional packaging was a "necessary evil" (the package was there to protect the chip, to redistribute the IO's to a pitch more suitable for the PCB and provide a mechanism that is easier to test), today's packaging can add significant value. There is an increase functional density and flexibility by providing a platform for heterogeneous design assembly. Where designs implemented in an SOC can become too large to yield satisfactorily and too difficult to implement on one process node, packaging now provides a platform to disaggregate the SoC die into its individual functional blocks and the use the package as a substrate.

Silicon-based substrates, 2.5D, and 3D stacking technology are blurring the design domains between classic IC design and advanced packaging. These "system" designs drive smaller form factors and lower costs, requiring early cross-domain planning and optimization tools. Not just a "nice-to-have", but a necessity in the design process; up-front planning effort can be more than half of the design process. Likewise, package designers were once left to resolve the constraints provided by the die designer and the constraints from the PCB designer, and would often be left to unscramble the connectivity.

Clearly, using an IC packaging design versus an IC tool that can manage a system is important. Let's now focus on making sure that the packaging design tool can meet all the silicon-based manufacturing requirements for implementation.

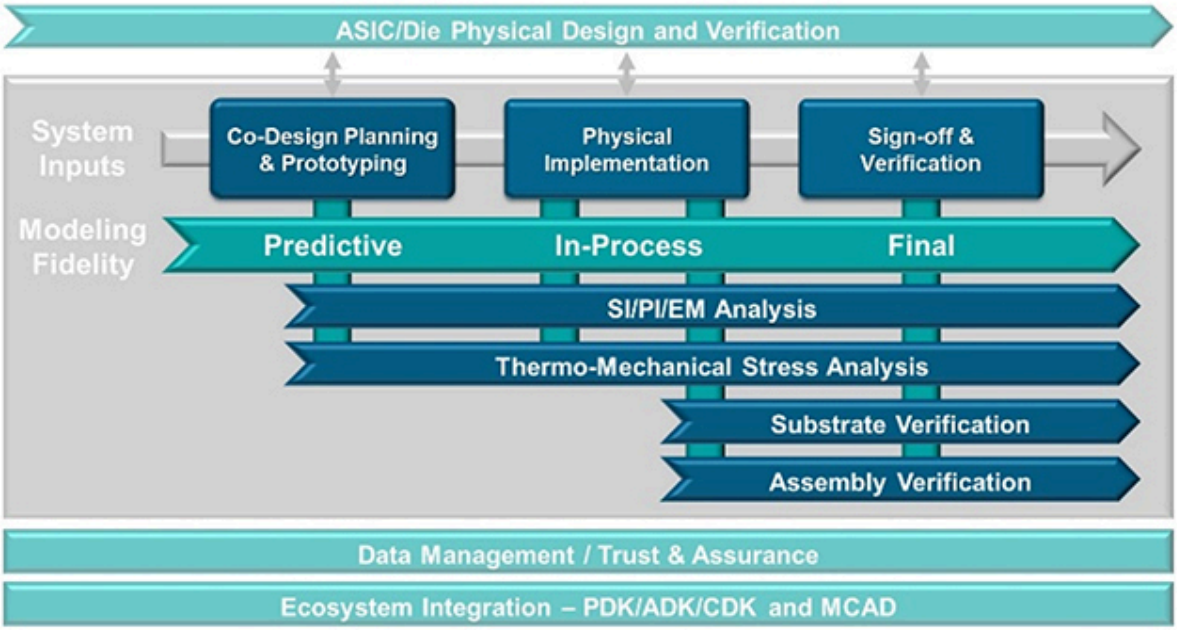

Figure 2. System co-design and analysis.

Implementing silicon design rules

Silicon substrates require specific design and manufacturing rules for their material properties and their manufacturing, just as there are specific requirements for the materials used in the various package technologies. Like die, silicon-based substrates have a specific set of design rules that are provided by the foundry or the manufacturer. These design rules govern the line width, spacing, and layer transition rules of each of the metal layers. There are rules that govern the localized density of metal on each of the layers of the design. There are rules that also govern how components are placed on the substrate, and how components are stacked and oriented within the design. There are also specific manufacturing requirements with respect to acute angles, overlap on the same layer, and overlap layer-to-layer within the design. All these IC layout rules can be managed in the IC packaging tool with either an on-line, batch, custom or a final artwork check. Obviously, the desire is to try to pull as many of those rules forward in the design process, to have them identified early rather than finding them at the end of the design process.

With respect to the IC design PDK (process design kit) provided by the manufacturer, there is a level of work that must be done to convert rules the silicon foundry provides to make them available in a packaging design tool. As these design domains have historically been different, it is not a 1-to-1 match. Although many of the rules can be directly implemented in the constraint system of the IC packaging tool, some of the rules must be implemented in other functions of the tool outside of the central constraint system (e.g., governing shape parameters). Most of these rules can be leveraged at the online DRC level and the rest of them will be implemented as a batch check or an artwork check. Silicon manufactures require strict PDK compliance and verification sign-off before a design moves to mask and manufacturing. The good news is that once the conversion is done, the IC packaging PDK can be leveraged on all future designs of the same technology.

Regardless of the manufacturer of the silicon-based substrate, GDSII or OASIS will be used as the manufacturing output for manufacturing in the silicon fab, and an artwork-based checker will be used for layout verification purposes prior to generating the masks; if not by the designer, by the manufacturer. To bring those checks earlier into the design process, the artwork checker (e.g., Calibre) can be integrated with the design tool. Cross-probing can be leveraged with xPDI such that those issues identified in the artwork checking tool can be cross-highlighted, verified, and corrected in the layout tool, and not just at the end of the design.

Another typical requirement of silicon and very thin organic substrate manufacturing specifications is localized metal density. This is not layer to layer, but intra-layer, localized metal density (Figure 3).

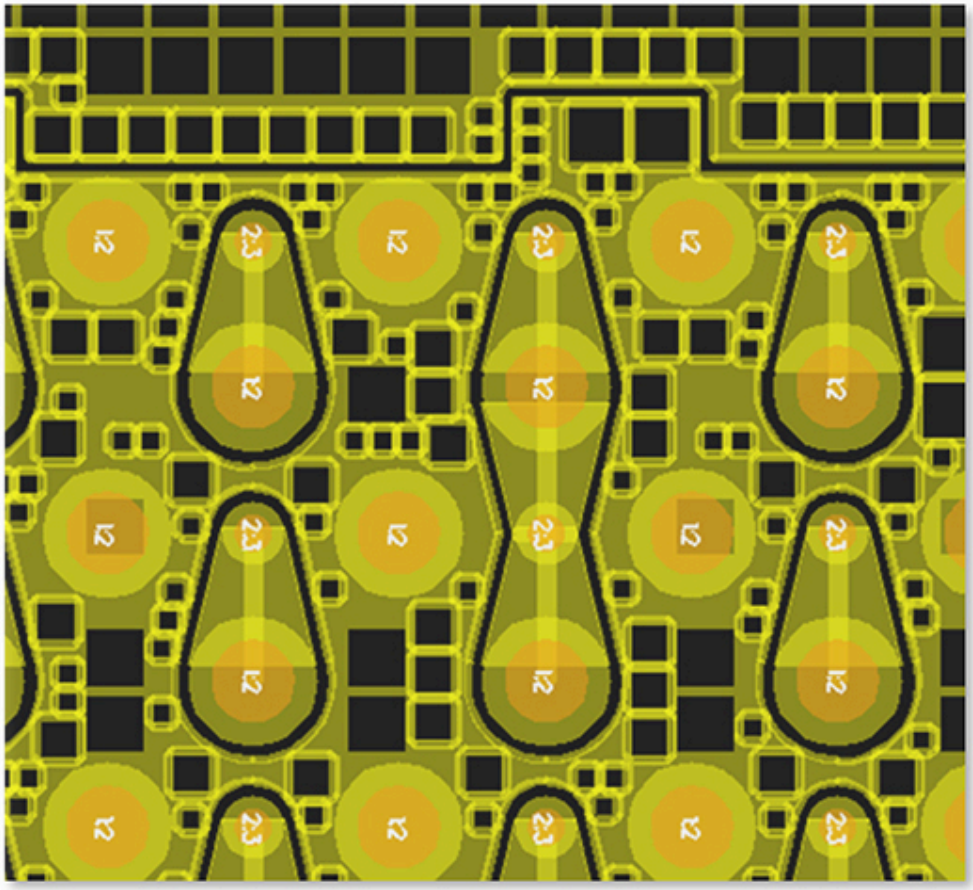

Figure 3. Density control.

Metal density has a direct impact on the process variation of etch rates and line widths on each metal layer. Due to these requirements, the packaging tool can be used to check compliance with the metal coverage and localized density rules. These density rules can be as simple as providing flooded planes in shielding areas around routing on a particular layer, to very localized density rules requiring, in some cases, perforating large via pads in the design because their density on the layer is an issue. Likewise, there's a significant emphasis on making sure that there are no acute angles within the design. There may also be layer-to-layer coincidence requirements (e.g., void to critical signal traces). Again, the good news is the IC packaging tools can address these. It is also important that the design tool can address these requirements while not being bogged down by the size and complexity of the database.

Depending on the requirements and the PDK for the IC manufacturing technology, arcs and circles and other typical substrate-based geometries will have to be implemented in silicon. Here is a merging of the classic orthogonal rules of IC design and the any-angle traces, arcs and circles common in packaging designs. These structures can be accommodated, either by limiting their use in the design itself (e.g. forcing orthogonal routing and using a 64-sided polygons rather than a circle) or, more commonly, having control over the way arcs and circles are converted into segmented polygons during artwork generation. There are very specific IC artwork rules that must be met with respect to the grid, acute angles, and spacing with no tolerances. (Figure 4)

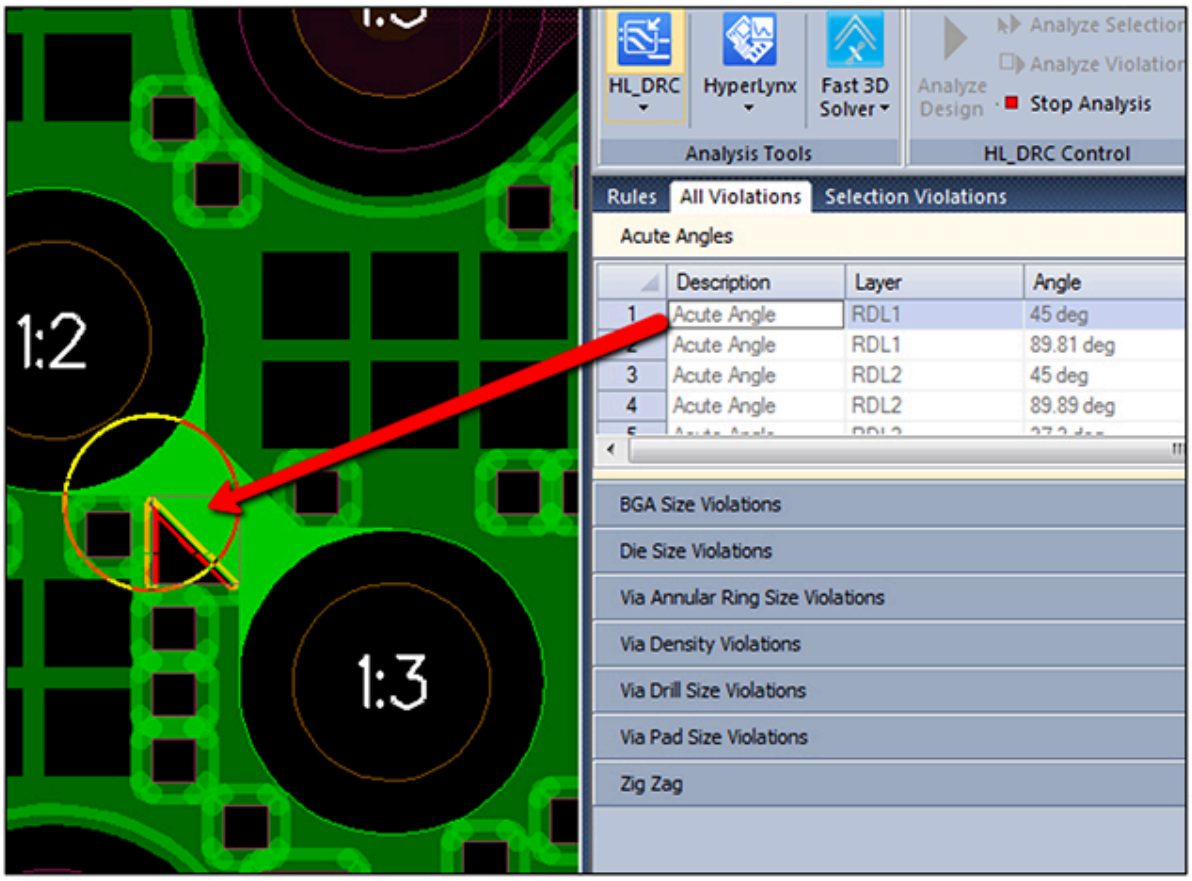

Figure 4. Acute angle violation.

Circular and any-angle geometries can generate thousands of GDSII artwork signoff errors if not processed and generated correctly.

Not only can IC packaging design tools meet almost all silicon based PDK manufacturing rules, they can also check additional requirements that have not historically been supported by IC design tools. The IC packaging design tools bring a wealth of additional capabilities and checks to the designer's toolset, specifically around filled shapes, differential pairs routing, and bus matching. The IC packaging designer can leverage these capabilities and checks across the interconnect of the overall system design on the silicon substrate.

There is also a wealth of interactive tools providing a better level of personal control in the implementation of the design. Digital IC design "place-and-route" tools rely heavily on batch type commands, and less interactive capabilities. IC packaging tools, relying on their PCB genealogy, provide a

wealth of interactive tools as well as the automation to implement the intent of the designer on the design canvas.

System verification

Because many of these silicon-based systems are multi-component, the packaging design flow also provides a tool – Calibre3DSTACK – to verify the system-level design. Calibre3DSTACK helps answer questions such as: are bumps in the correct location, do they have the correct assignment, are they oriented and aligned correctly, are there shorts or opens, and are the components oriented and placed correctly. These capabilities are not found in IC place-and-route tools, yet they can prevent costly assembly violations late in the process.

A previous white paper discussed the need and benefits of an assembly design verification process.[3] FOWLP packages and silicon substrates typically contain multiple devices and may have multiple substrates that are often stacked. These components are typically designed by separate designers and teams who may or may not communicate and collaborate efficiently and consistently with each other. When these designs are integrated, a number of system-level verification and validation procedures are required to ensure that they are connected correctly, both logically and physically. Ideally, the solution should be minimally disruptive to the overall design process while providing comprehensive DRC, LVL, and LVS verification of both the individual components, and more importantly, the final, assembled package.

Verification procedures must also be capable of managing the complexity and scale of the fully integrated 2.5D/3D assembly, where design pin count can easily approach one million pins. The required checks fall into two categories: physical (geometric) and connectivity. These checks are performed on the interface geometries between chip designs, including bumps, balls, through-silicon vias (TSV), and copper-

to-copper bonding. Dies from multiple processes can be supported with ease when using Calibre3DSTACK. It also provides independent verification, separate from the design tool's DRC engine, for greater confidence in result accuracy.

Conclusion

The IC packaging design tool set has matured to the point where it can address not only classic plastic, organic and ceramic packaging substrates but can also address silicon substrates driven by interposer and chiplet designs. In most cases system and packaging teams do not have to abandon their existing tool set to support these designs. In fact, the packaging design tool set can offer additional capabilities with respect to multi-component system design and component stacking better than an IC layout tool.

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