Viaffirm Temporary Bond and Fill for Glass Interposers: A Simplified Path to Copper-Filled Through-Glass Vias

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Introduction:

Advanced packaging relies heavily on silicon interposers and on organic materials such as printed circuit boards (PCB). Printed circuit boards represent a low cost, scalable platform. However, they exhibit rough surfaces, limiting the resolution of metal traces, and are subject to dimensional changes from environmental factors including temperature and humidity. Silicon for interposers, at the other end of the spectrum, offers excellent surface properties and dimensional stability, but is more expensive. Silicon also is not a true insulator even in its intrinsic form, leading to loss[1] and lower performance for high frequency operation.

Property	Aluminoborosilicate Glass	High Purity Fused silica
Modulus (GPa)	74	73
CTE (ppm/°C)	3.2	0.5
Dielectric constant	5.3	3.8
Loss Tangent	0.006[a]	0.0004[b]

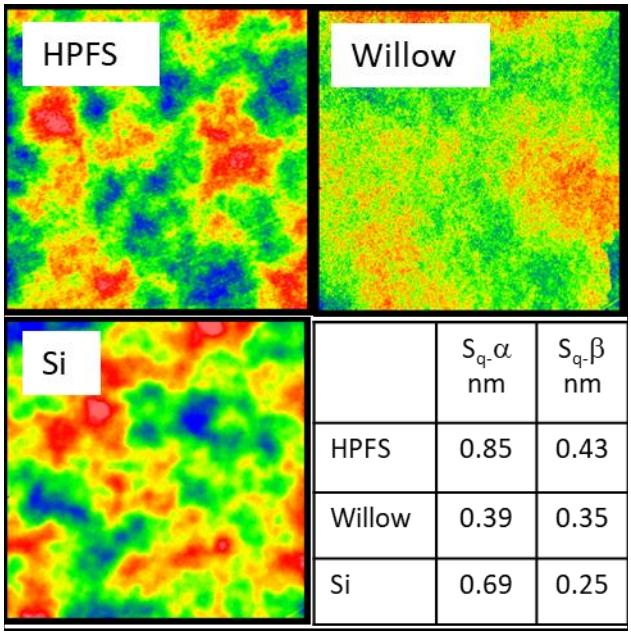
Table 1*: Properties of aluminoborosilicate glass and high purity fused silica. a: 10 GHz, b: 100 GHz*

Glass substrates offer a compelling alternative for packaging based upon properties and manufacturability[2].

Table 1 presents data for two common glasses available as packaging substrates. High purity fused silica (HPFS) as its name implies is pure silicon dioxide. It has a low coefficient of thermal expansion (CTE), and a remarkably low loss tangent for high frequency use. HPFS however has a softening temperature, indicative of the temperature required for production, around 1600 °C. As a result, HPFS wafers are produced in a process similar to the production of silicon wafers in which cores of glass are sawn, ground, and polished to form wafers. Aluminoborosilicate glasses, such as Corning's Willow®, are an alternative with a good blend of performance and manufacturability. These glasses have a softening point around 1000 °C, which permits processing into sheets and webs. While the Willow has a higher CTE than HPFS, the CTE is well matched to silicon, leading to good synergy during processing with silicon handles and also reliability as final interposers with silicon die attached.

Both types of glass offer bulk resistance greater than 10^{10} Ω-cm, much higher than its silicon counterpart which can only attain about 10^{6} Ω-cm. Mechanically, they have high strength with a Modulus of elasticity near that of silicon. They can thus be produced in a form with low warp and low total thickness variation (TTV), essential to lithography of fine lines and spaces. Furthermore, glasses are chemically robust, resistant to moisture in operation and aggressive chemistries during processing. This

combined with high temperature resistance renders them compatible with many of processes normally reserved for silicon and outside of the range of those available for PCB materials.



	S_q-α nm	S_q-β nm
HPFS	0.85	0.43
Willow	0.39	0.35
Si	0.69	0.25

***Figure 2**: Optical profilometry scans of semi-conductor grade wafers of HPFS 7980, Willow glass, and silicon. The inset shows rms roughness (Sq) for different spatial frequencies as described in the text.*

The smooth surface of glass substrates, comparable to that of silicon, is an attractive attribute when considering glass in processes developed for silicon interposer fabrication. Fig. 1 shows optical profilometry of surfaces of an aluminoborosilicate wafer (Corning Willow, 200um thick), HPFS 7980 produced by wire saw and grind/polish (Corning), and a typical silicon wafer. The rms roughness (S_q) is reported filtered for two spatial frequency ranges: S_q-α, showing special frequencies with a period below 400um, and S_q-β, showing spatial frequencies with a period a period below 50um. The data in Fig. 1 shows that all of these materials have RMS roughness well below 1 nm. The data also shows a very smooth surface of the melt formed Willow glass with low Sq values at both spatial frequencies, an indicator that excellent surface quality can be obtained even with high volume glass production methods.

Temporary Bonding for Robust Thin Glass Handling

Many applications for glass require thin substrates, below 200 μm. During fabrication flexibility can lead to excessive sag, resulting in incompatibility with process tools, and breakage. As an example, a 100 μm thick 300mm glass wafer will sag about 15mm when held from two edges. A well-known approach to help with substrate flexibility is to use temporary bonding of a thin device wafer to a handle. The handle wafer is normally a glass or silicon wafer thick enough (0.5 to 1 mm) to support the device wafer through processing. The device wafer is held securely, eliminating excessive sag, and in the case of a silicon handle wafer, offers fabrication tools a bonded wafer pair that has the shape and opacity of a standard silicon wafer.

Some temporary bonds involve attachment to a handle with a polymeric adhesive. While these approaches can securely bond a thin device wafer to its handle, polymers have low resistance to aggressive chemistries or temperatures over 250 °C. Additionally, the polymer layers are typically thick (10-20 μm) and therefore their thickness variation can add appreciably to the overall bonded pair total thickness variation (TTV). Importantly for through-glass vias (TGV), polymeric bonding materials can wick into open vias during the bonding process when the polymers are fluid, thus fully or partially blocking the vias and harming the seed and electroplating that are essential to an advanced glass process.

The Viaffirm® temporary bond [3,4,5] offers a solution without these drawbacks. It leverages a thin (<1 μm) inorganic bonding layer that is very uniform in thickness and thus does not contribute to TTV of the bonded pair. Because it is inorganic, the layer is very resistant to temperature, surviving anneals as high as 450 °C, as well as process chemistries involving acids, bases, and even megasonics treatments. Fig. 2 shows a process flow using Viaffirm bonding. Glass with TGV (unfilled) can be bonded to a handle wafer, silicon or glass, without concern for contamination of the TGV features. The bonded pair can be processed, including TGV fill, removal of overburden, anneals, and redistribution layer formation, followed by a simple mechanical debond. As such, the Viaffirm bonding approach enables a thin glass device bonded to handle to be processed with almost any convention fab process, providing a route to thin glass processing without the need for capital-intensive equipment modifications.

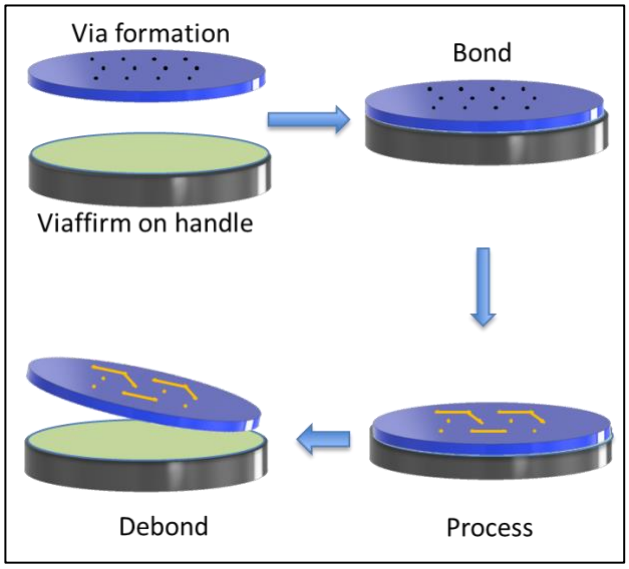


Figure 3: *Viaffirm process flow*

Via Formation in Glass Substrates

Vias can be made in glass substrates by dry and wet etching, and laser-based processes. Methods that involve photolithographic patterning followed by plasma dry etching [6] can have the advantage of being able to process full wafers at a time, but are limited in etch rate and thus not practical as via depth exceeds 50 μm. Laser-based via processes have gained in importance in recent years. Laser ablation [7] can be used to drill vias either by direct ablation or trepanning to cut out a via hole. Such methods rely on direct material removal, requiring many laser pulses to gradually form a via. The laser-based removal is slow, and results in debris generation.

Laser-assisted chemical etching [8] adapted to via formation in glass is an attractive alternative, combining the flexibility of a fast laser process with the cleanliness and throughput of wet etching. In the laser-assisted etch, a laser pulse modifies glass in localized region, increasing its local etch rate significantly over the etch rate of surrounding bulk glass. The laser drilled substrate is then etched in order to open up a via pilot hole, allowing rapid simultaneous etching of larger numbers of vias on a substrate, and multiple substrates at a time.

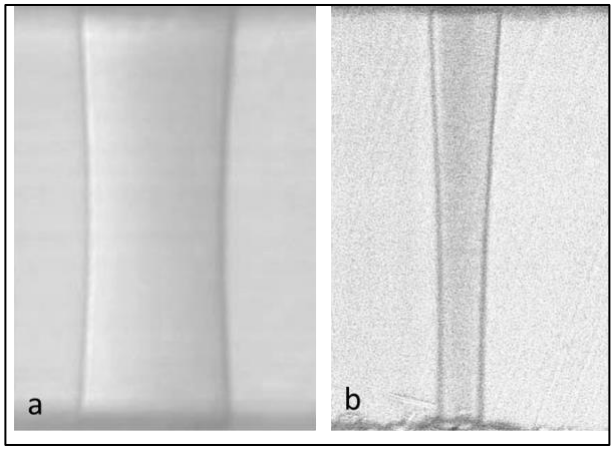


Figure 4: *Examples of (a) a symmetric via having a 35 μm end diameter in 100 μm thick glass via ; (b) a tapered via having a 30 μm top diameter / 20 μm bottom diameter in 175 μm glass.*

We have used laser modification combined with novel etching approaches to produce a wide range of via shapes from the same initial laser pilot hole conditions. Fig. 3 shows examples of two limiting morphologies, a symmetric via (Fig. 3a) and a tapered via (Fig. 3b), imaged by microscopy through a polished glass edge. The symmetric via shown has a small amount of hourglass (reduction in diameter at the center of the via). This hourglass can be tuned, or removed resulting in a columnar via. The columnar via is of interest as it has a constant cross section, leading in the case of a filled via to a constant resistance along the length of the via. Alternatively, a tapered via is possible as shown in Fig. 3b. While the tapered via does not have a constant cross section, it can be more suitable for via fill seed and plating processes.

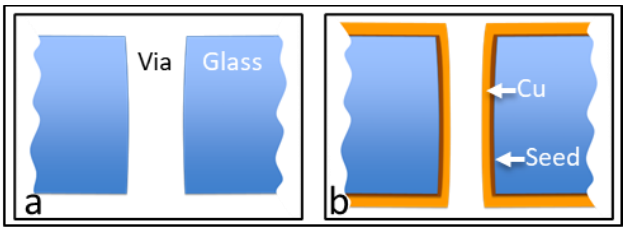


Figure 5: *Example of 2 sided conformally coated via. (a) pre-metallization; (b) Post metallization with dark region representing the seed layer.*

The laser-based etch process also results in excellent via size uniformity, because while the laser drill process produces a small pilot opening, the highly uniform wet etch process dictates final via size. As an example, a nominal 30um diameter via in Willow glass over a 200mm wafer has a coefficient of variation of diameter on the order of 1.5%. This number is reduced even further for HPFS, where the slower surface etch rates lead to coefficients of variation closer to 1% for a similar via.

Via Fill & Performance

There are several approaches to copper vias in thin glass. Fig. 4 illustrates a conformal plating approach in which the via is metallized from both sides [9]. In this approach, a seed layer (shown as the darker area in Fig. 4b) is applied on the glass by either physical vapor deposition (PVD) or electroless processes. The latter is often used in order to achieve seed layer on both surfaces of the glass without the need for a two PVD steps. The substrate is then electroplated, normally in a double-sided process, with a conformal growth chemistry as illustrated in Fig. 4b. The resulting coated via is not fully filled, and so is not intrinsically hermetic. Several techniques exist to seal the opening in the vias, with polymeric materials, for example. While some degree of hermeticity can be obtained with these methods, polymeric

materials experience appreciable permeation by water and gaseous species, and will also not have compatibility with high temperature or aggressive chemistries downstream.

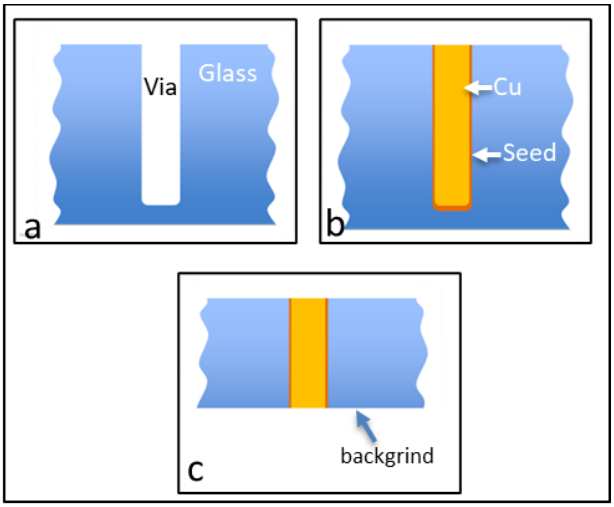


Figure 6: *Blind via fill with backgrind / polish. (a) pre-metallization; (b) post via fill and CMP; (c) post-backgrind, with via backside reveal*

Another approach to via fill, with parallels to silicon TSV, is shown in Fig. 5. In this approach, blind glass vias are formed in thicker glass, typically 500 µm or thicker. Seed layer deposition (shown as the darker area in Fig. 5b) can occur with convention vacuum deposition methods. Most commonly, PVD is used, with attention to obtain good metal coverage throughout the via walls. Metal organic chemical vapor deposition (MOCVD) can also be applied. While generally a more expensive process, it can produce excellent conformal coverage allowing compatibility with steep via walls and reentrancy. After seed electroplating, using standard bottom-up chemistries borrowed from silicon TSV approaches, produces a filled via.

Also in analogy to silicon processes the thicker glass is thinned by back-grinding/polishing processes to reveal the via and obtain the desired final substrate thickness. While the process produces a filled via with excellent hermeticity, the need to grind and polish increases cost and reduces yield, and may result in a poorer backside surface than the glass intrinsically possesses. Additionally, the need to have a deeper via than the final one requires a deeper via formation and an incremental amount of plating.

A third alternative is shown in Fig. 6, leveraging the temporary Viaffirm bond. In this approach, a blind via results from assembly of the glass via (preformed) to the handle substrate (Fig. 6a). The via depth is only that of the final product, and can be seeded using standard PVD seed approaches pioneered by TSV work. Similarly, the via can be filled void-free using available bottom-up fill chemistries, as illustrated in Fig. 6b, with dark areas representing the seed layer. The seed layer is designed to promote good adhesion to the walls of the via while yielding a lower adhesion to the handle substrate.

Thus far, the processing and handling is similar to the blind via of Fig. 5. After this stage, however, the handle substrate can be removed (Fig. 6c) by simple debonding to yield a finished substrate. As discussed later, the debond yields excellent planarity of the lower via surface, and a clean substrate ready for subsequent process steps.

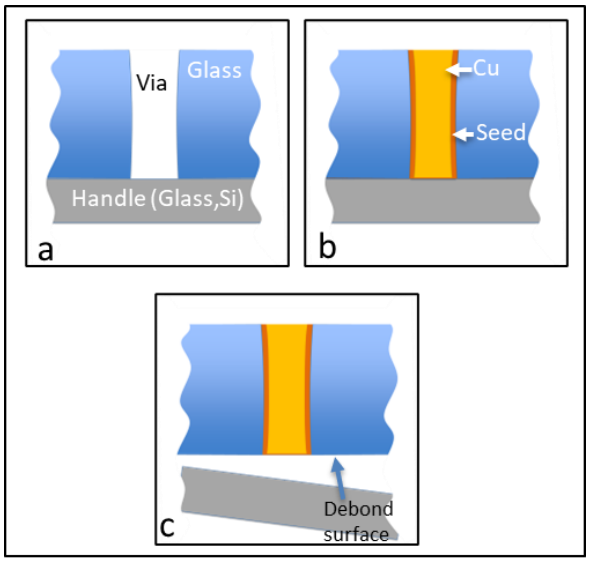


Figure 7: *Viaffim bond and fill. (a) Pre-metallization; (b) post-via fill and CMP; (c) simple debond for via reveal.*

Fig. 7 shows several copper filled vias produced by the Viaffirm bond and fill process, demonstrating the range of compatible morphologies and sizes. Fig. 7a is a slight hourglass via in 100um thick Willow glass, having a top diameter of 35um (~3:1 aspect ratio). Fig. 7b shows a via also of 35um diameter, now in 150um thick HPFS, exhibiting columnar shape. The laser assisted chemical etch process can also produce higher aspect ratio structures. Fig. 7c shows a 14um via in 110um Willow glass (aspect ratio ~8:1), also fully compatible with a bond and fill approach. The void free fill in these various vias results from the ability to use conventional seed and plate techniques for bottom up via fill.

All of the vias shown in Fig. 7 are still attached to the handle substrate. For Figs. 7a and 7c, the handle is silicon, seen as lighter grey in the images. In Fig. 7b, the handle is HPFS, so no contrast is visible between the device and the handle. Substrates at this stage would normally move onto various process while still bonded: CMP to remove the overburden, annealing, and RDL formation. Once top surface processing is done, the substrate can be debonded with a simple mechanical process.

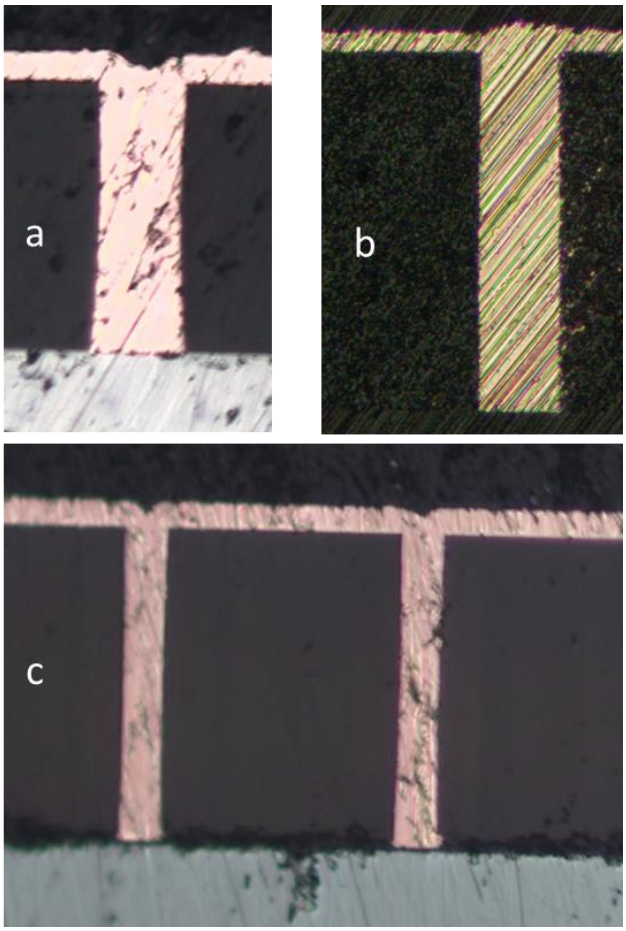


Figure 8: *Vias with copper metallization by the Viaffirm bond and fill approach. (a) a 35 μm hourglass via in 100 μm Willow glass; (b) a 35 μm columnar via in 150 μm HPFS; (c) a high aspect ratio 14 μm via in 110 μm Willow*

The cleanliness and planarity of the debonded surface are critical to eliminate the need for additional steps prior to second-side processing. Polymeric temporary bonds usually leave residues that require solvent or mechanical removal. In contrast, the Viaffirm bonding material, applied only to the handle wafer, remains exclusively on the handle after debond regardless of processing.

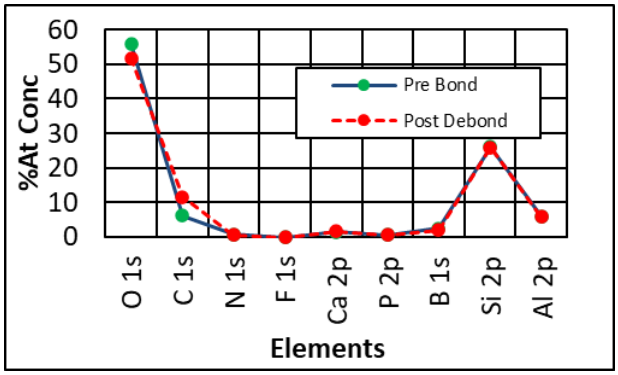


Figure 9: *XPS data for a clean glass wafer (green circles) and the same wafer after bond and debond (red circles)*

Fig 8 demonstrates the cleanliness of a debonded wafer with x-ray photoelectron spectroscopy (XPS) data taken on a glass device wafer prior to bonding with Viaffirm and after debond. XPS is a very surface sensitive technique, resolving atomic constituents mainly with about 10nm of the surface. As such, the measurement pre-bond shows oxygen and silicon from the device glass, as well as peaks from calcium and aluminum present glass. Few additional constituents can be seen on the wafer aside from small amount of adventitious carbon. Importantly, after debond the XPS signature of the glass surface is almost unchanged, excluding a small growth in the carbon peak. Such movement of the carbon peak is also seen on clean glass, within the range expected for adventitious carbon. Residues of any form after debond would show their composition, and would mask the glass silicon an oxygen peaks. The lack of these effects suggests and extremely clean surface after debond.

Also important is planarity of the via bottom after debond, shown in Fig. 9. In effect, during the via process the growing copper seed and fill are molded by the handle glass, and thus peel away with low roughness. We see lack of planarity in these regions on the order of 100 nm, but within the exposed copper the roughness by optical profilometry is on the order of 1 nm, comparable to that resulting from CMP. The combination of the low surface contamination and smooth copper via lead to a surface that is readily processes after debond.

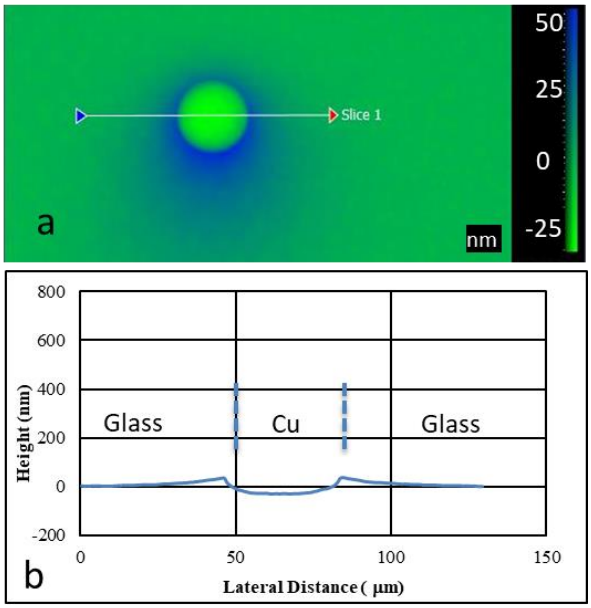


Figure 10: *(a) Optical profilometry scan of a via bottom after debond; (b) Height trace through the debonded via, showing a smooth surface with low roughness*

Finally, hermeticity is another feature resulting from this architecture that relies upon proven TSV seed and fill approaches. As an example, we have demonstrated hermeticity in 100 µm thick Willow glass containing 25 µm vias after annealing as high as 450 °C.

Outlook

Glass offers many advantages in next generation packaging. It combines mechanical and surface properties of silicon with insulating and dielectric loss properties as good or better than the best specialized PCBs. As communication frequencies extend past 5G to above 100 GHz and beyond, and with constant pressure to

reduce size, weight and power, the properties of glass become essential. Adoption of glass is now limited by supply chain: fabrication equipment interface and substrate handling mean that new solutions are needed to easily integrate glass into existing fabs.

The Viaffirm bond-and-fill solution addresses these concerns, providing both a handling solution the allows integration into existing process flows, and a novel method to produce filled TGV's that actually reduces process complexity.

References

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