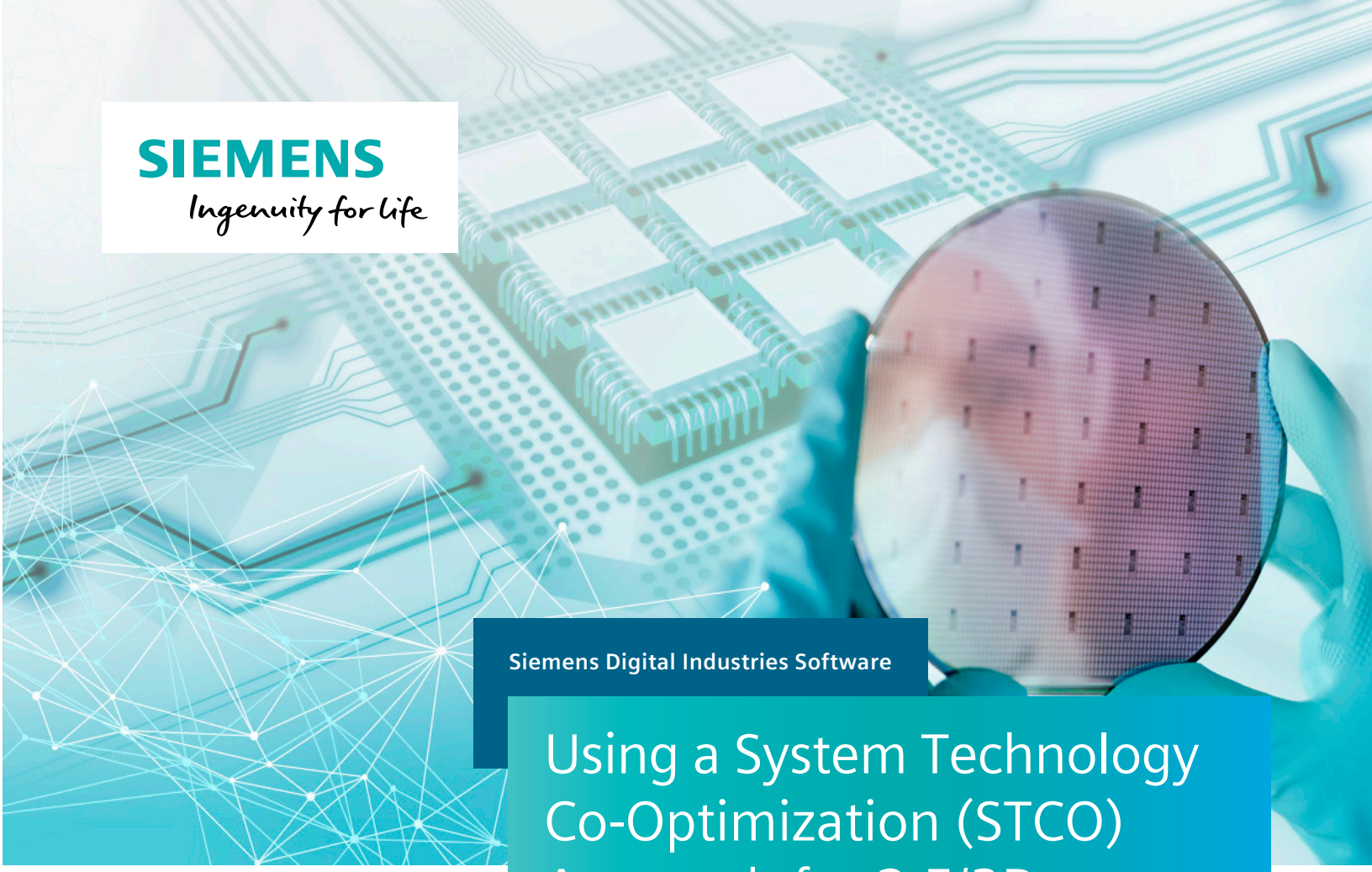

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Using a System Technology Co-Optimization (STCO) Approach for 2.5/3D Heterogeneous Semiconductor Integration

Executive summary

With the economics of transistor scaling no longer universally applicable, the industry is turning to innovative packaging technologies to support system scaling demands and achieve lower system cost. This has led to the system technology co-optimization (STCO) concept, where a SoC type system is disaggregated, or partitioned, into smaller modules (also known as chiplets) that can be asynchronously designed by dispersed teams and then combined into a larger, highly flexible system using chiplet-based package design, which may involve 3D packaging.

Per Viklund

Introduction

Moore's law is increasingly difficult to maintain. With the economics of transistor scaling no longer universally applicable, the industry is turning to innovative packaging technologies to support system scaling demands and achieve lower system cost. This has led to the system technology co-optimization (STCO) concept, where a SoC type system is disaggregated, or partitioned, into smaller modules (also known as chiplets) that can be asynchronously designed by dispersed teams and then combined into a larger, highly flexible system using chiplet-based package design, which may involve 3D packaging.

With this greater flexibility comes several additional challenges in the form of power integrity, signal integrity, thermal performance, warp, and mechanical stress. Finding and having to fix such issues late in the design cycle becomes exorbitantly expensive. This paper proposes a shift left approach where analysis is performed very early, and the results are used to drive design decisions as well as make corrections to mitigate the risk of verification failures later in the design flow. We will examine how such early analysis in complex high density advanced packaging (HDAP) flows enables designers to spot potential issues early to avoid built-in constructs that cause design failures and require major redesign work.

While verification analysis of a completed design can offer very accurate results, it is way too late in the process to provide value. The shift left approach entails applying multi-physics analysis very early in the design process: at the prototyping and design planning stage where very little is known about the design. We will show how a minimum of input still provides enough detail to drive a left shift process. This paper focuses on power and signal integrity prototyping in STCO HDAP, but the approach applies equally to thermal, warp, and mechanical stress.

What is STCO?

The answer is often different depending on who is asked or from which perspective the question is asked.

At a very high level, it is a process or methodology to partition or disaggregate complex SoC like systems into smaller partitions that can be designed asynchronously and concurrently. This allows each piece to be processed using the optimal process for that piece, and then all the pieces are reassembled through 2.5/3D packaging, typically utilizing a silicon interposer.

If this is STCO, what have we been doing thus far? The answer is device technology co-optimization (DTCO). When we move from device scaling to system scaling and from device packaging to system packaging, we transition from DTCO to STCO.

It's important to understand that DTCO and STCO are not products or tools provided by EDA vendors or developed in house. Both are methodologies used to optimize a "design" and help manage the increasing complexity and cost that follows design scaling [1]. While there are similarities, STCO starts earlier and higher up in the design process and focuses around disaggregating a system so the pieces can be built at a lower cost and be put together in a way that supports higher performance.

In both methodologies we focus at making educated design decisions very early to avoid costly issues late in the process. In DTCO, we utilize knowledge about both the design and technology to help converge a design to a solution. With STCO, we add knowledge about the system (thus system technology co-optimization). The gains are P3: performance, power, and price (cost).

Before we proceed, we need to clarify terminology: the difference between what we mean by "chiplet" in the context of chiplet design and what it means in the context of STCO. In chiplet design, chiplets are standard, reusable, "off the shelf," fabricated semiconductor blocks with standard interfaces—such as AIB (advanced IF bus), BoW (bunch of wires), OpenHBI, and others—that enable easy integration. In STCO, chiplets may not be off the shelf but instead result from system partitions that may be design specific. Nothing prevents reuse in this case, but reuse may not be the objective.

STCO can be applied to a chiplet design but disaggregating an SoC results in functional blocks that don't necessarily need to be chiplets— in other words, modules with standard interfaces. An STCO chiplet can be simply a "module" designed to only operate with another specific "module." There are still many design options (in both cases) and both benefit from an STCO shift left process.

Early multi physics analysis for STCO

STCO brings many benefits but also new challenges. It enables teams to work in a concurrent yet asynchronous manner using dispersed design teams. Each design fraction can be worked on concurrently by different teams independently of each other. This allows us to choose the optimal processes for each fragment of the design. However, to do this, the data for all the fragments must come together at some point, and this point is in the package planning. This is when we reassemble the disaggregated SoC functional blocks (chiplets) and examine the packaging options.

The partitioning, or disaggregation, that was made will impact our ability to build a working package as well as package costs. It's clearly important how that disaggregation is made, yet it's made by teams that generally don't have the downstream insight or means to consider the packaging impact of their decisions.

This is the main challenge we are looking to solve: How to reintegrate the design fractions into an early package prototype that has enough information to drive multi-physics analysis to help guide the partitioning. This includes evaluating the connectivity between design fractions. This analysis gives us critical information. By feeding that gained knowledge back to the silicon team, they possess invaluable information to help reconsider the partitioning (if needed).

It would be easy if partitioning was function block based. Designers may look at a block diagram of the design and make each block a design fraction. Unfortunately, it's not quite that simple with STCO.

We need to consider things like the performance of each fraction and how it communicates with other fractions at a more detailed level. For example, will 3D stacking a block result in a performance and power gain or cause a thermal issue?

We are looking to get a higher performing, lower power solution. Regardless of how we partition, there are always multiple partitioning and integration options: finding the right one is what STCO is all about. There are likely more than one good solution, so to find out which of these is best, we build a package prototype that we can use to analyze and weigh each partitioning option of interest.

We build the package prototype incrementally and refine it as data becomes more refined over time (Fig. 1).

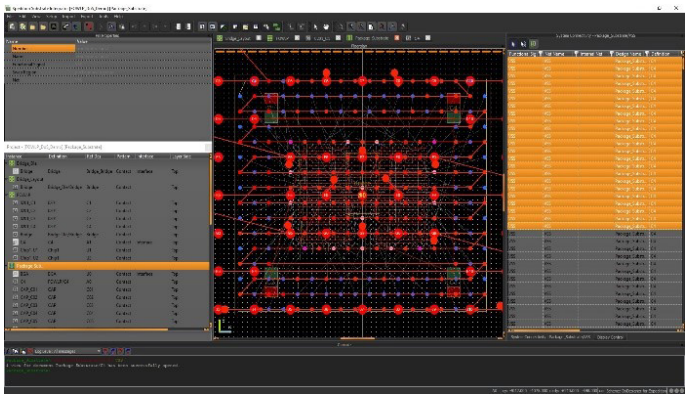

Fig. 1 Early package prototype

At the package prototype level, we are first able to estimate power integrity and signal integrity, so the initial best effort partitioning needs to become a package prototype.

The package prototype is just what the name implies, a model of the intended package, not a detailed implementation. We know the size of the design's functional blocks or chiplets. We know their signals, and through a SystemVerilog description of the system, we know how they connect to each other. Using a Verilog visualization tool, we get a clear overview of the circuitry, as it displays a graphic representation of the Verilog code (Fig. 2).

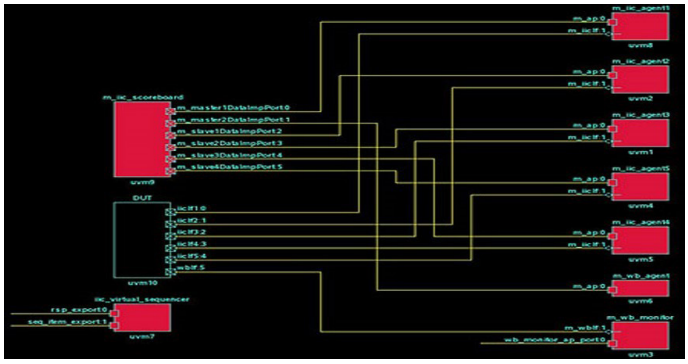

Fig. 2 Visualizing SystemVerilog in graphic form

We may —or may not— have physical die information through LEF/DEF at this stage, but if we have, we can use it for a more detailed prototype.

We can now start by calculating the number of power and ground bumps we need for each module and build a preliminary bump map. This data is enough to take our package prototype into power integrity tools and do some very early, preliminary analysis that will tell us if it looks OK or if we have any trouble areas (Fig. 3).

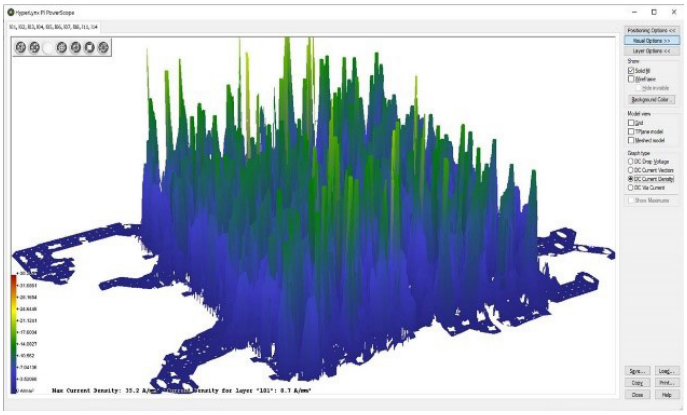

Fig. 3 Power integrity simulation at the prototype level

We would also characterize the signal I/Os and run preliminary signal integrity analysis to see if various 3D stacking configurations can give us the results we are looking for and, more importantly, if it fails at this level.

Essentially, we are packing more silicon into smaller area by extending along the Z axis: Volume. It's obvious that the more we integrate into a small volume, the greater the chances that we will create a thermal problem. For that reason, early thermal estimation is as vital as signal integrity and power integrity. Since we are still early in the design phase, we cannot do a detailed simulation of any domain, but again, we can get quite far with what we do know. This is because the package prototype gives us the physical representation and the silicon design gives us an estimate on power, and we feed these into a 3D thermal simulator. 3D because these packages are truly 3D structures, and even though it is an early estimation, to simplify the package as a 2D structure is too trivial to be of value (Fig 4).

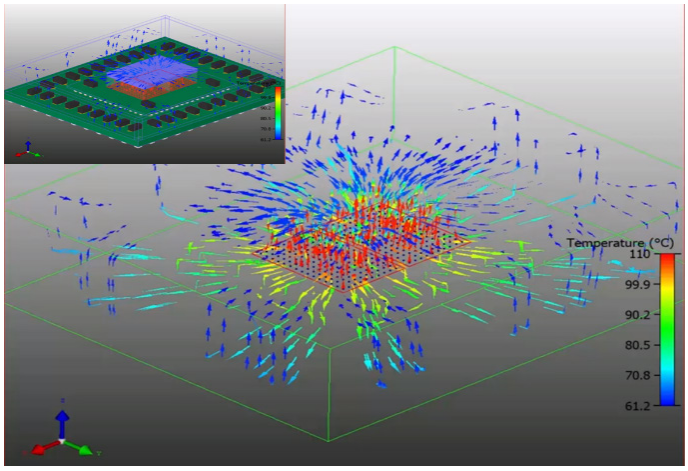

Fig. 4 Thermal prototyping

We have covered signal integrity, power integrity, and thermal, but since we have a complete 3D assembly model —aka a digital twin— we can, when there is a need, expand early analysis into mechanical stress, warping, die attach failures, metal cracking, and other physical effects. The key is that we use early IP partitioning to create a package prototype, perform meaningful simulations very early, and use the results to adjust partitioning.

Early analysis is not a replacement for more accurate simulations or package and assembly level verification— and as systems get more complex in every aspect, a final, 3D, full assembly verification is the only way to ensure success. As part of the early planning and creation of the 3D package assembly model, we also define the logical connectivity model that can be used to drive early verification, which can happen before physical design (place-and-route) of the package assembly. This enables executing multiple verification runs en route to completion — which will help identify issues early that could derail or delay a project if found at tape out. Early is the shift left keyword.

How do we know that the package prototype is correct? We can take Verilog from the package prototype and use simulation to compare that against the original Verilog.

Conclusion

Early system partitioning and integration planning can have a profound impact on physical implementation in areas like power integrity, signal integrity, thermal performance, package warping, and mechanical stress. If partitioning and integration are not properly managed, they can make the entire product fail. In the partitioning process, it's not possible to see the physical consequences of a partitioning option. As this is early in the design phase, not enough details are known to make accurate detailed simulations, but there is enough to make fast, approximate analysis to help catch issues.

We are suggesting a process where ASIC partitioning is fed forward to package prototyping early so the physical effects can be analyzed. Solutions derived in package prototyping, guided by multi-physics analysis, is handed back to the silicon teams to help drive IP partitioning and enable the IC design teams to make better, more educated decisions at a stage where partitioning can be changed before the design is too far along and costs of fixing problems become prohibitive. In other words, make decisions earlier: shift left.

References

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