OPTIMIZING YOUR SoC OR ASIC TO DESIGN PCBs MORE COST EFFECTIVELY

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I C T O P C B

W H I T E P A P E R

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Many high-performance systems today use custom ASICs or SoCs to provide the necessary computational power and data bandwidth demanded by their host system, whether it's a network storage device, network data switch, complex industrial equipment controller, or a critical core module of a defense system. And they are not getting any smaller or slower as silicon process nodes shrink and memory demands continue to grow. The result can be a nightmare for the system PCB design team who have to integrate this often huge (size and number of PCB level connection balls) device while maintaining the overall integrity of the PCB-based system while ensuring signal layer count and overall PCB size stay within system and cost constraints.

This paper demonstrates the causal relationship between PCB Signal to ASIC/SoC pin assignment and the product's profit margin. It also defines opportunities for generating significant competitive advantages without incurring significant time or cost penalties.

DETAILING IMPACTS TO PROFIT MARGIN

Most Engineering and Product Managers would be stunned to learn that every PCB signal to SoC/ASIC pin assignment has a direct impact on their product profit margin. Each time a PCB signal is assigned to a SoC/ASIC Package pin both the SoC/ASIC and PCB design domains are impacted. While the impact of any single decision may be minimal, the impact of several thousand such decisions can have a material impact on the cost, performance, and reliability of the design. Within each design domain, both the functional and physical aspects of the SOC/ASIC-PCB interface are available for alteration. By confining our focus to the physical changes to the PCB interface, we can simplify the challenge without losing focus on product profit margin.

Anytime a PCB signal is moved from one device pin location to another device pin location, the PCB trace length, PCB via count, and routing congestion are impacted. In the case of PCB trace length and routing congestion, the impact is visually obvious, as seen in Figure 1.

The two PCB signal-to-device pin assignment options depicted in Figure 1 clearly demonstrate how the location of the physical connection point to the SOC/ASIC package impacts the length of PCB traces. In this example, the PCB trace length was reduced by 50% and routing congestion and via count were reduced.

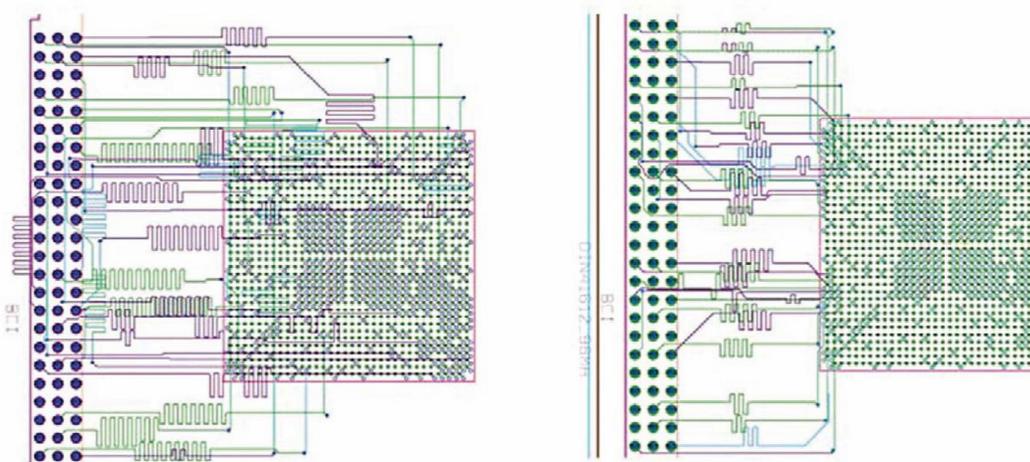# PCB Signal Location Impacts Trace Length

Figure 1: The location of the critical signal/pin assignments impacts the overall trace length, easily seen in these two views

Trace length impacts signal propagation delay across the trace. By reducing trace length by 50%, propagation delay was reduced by 50% and the maximum operating frequency of a signal operating across these traces was increased by 100%.

Minimizing trace crossover through the flexibility of PCB signal to SOC/ASIC pin assignment increased the reliability of our PCB system design too, as PCB vias are susceptible to vibration and consequently are potential mechanical and electrical failure points. While the impact to routing congestion is visually obvious, attributing statistical characteristics to routing congestion requires a careful measurement of the surface area consumed by both signal assignment options. In our trivial example routing congestion was reduced by approximately 20%.

Clearly, PCB signal to SoC/ASIC pin assignment impacts:

- PCB trace length

- PCB propagation delay and signal quality

- PCB reliability

- PCB routing congestion

ACCELERATING SYSTEM CONSTRAINT CONVERGENCE

How much time is spent in the design cycle "tuning" the PCB design to meet timing and signal integrity constraints? While "the shortest distance between two points is a straight line" is accurate, it is also true that the shortest distance is achieved when the "two points" are moved as close to each other as possible, and with differential signaling or matched length interfaces, the length relationship between the signals is managed. The magic of custom SoC/ASIC devices in system PCB designs is that one of the two points in an electrical connection is flexible.

Instead of spending excessive amounts of design time "tweaking and tuning" the PCB design to meet system constraints by altering component placement, component rotation, PCB layer stackup, PCB signal layer pairs, trace routing, and possibly PCB manufacturing materials, the pragmatic approach is to leverage the inherent flexibility of the SoC/ASIC custom packages. By first minimizing the connection distance between the SoC/ASIC and the other components on the PCB system, the time spent "tweaking and tuning" can be reduced by 20%-50%.

ACCELERATING SYSTEM PHYSICAL DESIGN AND
MINIMIZING MANUFACTURING COSTS

Likewise, a high-quality SoC/ASIC-PCB interface design can reduce the amount of design cycle time spent routing traces on the PCB from 25% to 50%. One critical value delivered to the system design by custom package flexibility is reduced routing congestion which creates additional signal-layer pair surface area that can be used for routing additional traces. When the routing congestion trend is applied to high pin density custom packages it is quite possible that a high-quality SoC/ASIC-PCB interface will reduce the number of signal layer pairs required to implement complex systems. The resulting savings in manufacturing costs from a single signal layer pair reduction are significant for moderate production volumes; for example, going from an 8-layer PCB to a 6-layer PCB can reduce fabrication costs by 30%.

Leveraging the flexibility of ASIC? devices to reduce routing congestion is a proven method for taking an "un-routable PCB" and transforming it into a "routable PCB" without adding to PCB manufacturing costs. The opportunity often overlooked is the time required to determine that the current PCB layer stackup does not provide the trace routing surface area necessary to complete the design…the amount of time before the declaration of an "un-routable PCB."

PROFIT MARGIN IS THE LAST DOMINO IN THE IMPACT DECISION CHAIN

The logical decision-impact chain from SoC/ASIC-PCB interface design to product profit margin is a simple "domino cascade." The dominos fall whether or not the engineering community is consciously aware of their linkage. The simple truth is that many system design teams are unaware of the decision-impact chain simply because it crosses design domain boundaries and creates clashes with historical and cultural design processes.

UNDERSTANDING THE BARRIERS TO PCB OPTIMIZATION

If the flexibility of SOC/ASIC custom devices may be used to optimize PCB designs, why is this flexibility so infrequently leveraged by design teams?

- Design Complexity

- Risk Analysis and Aversion

- Design Team Organization and Silos

- Traditional Design Processes

- Historic Design Support Infrastructures

- Time to Market Constraints

- Availability of Tools

DESIGN COMPLEXITY

In fundamental terms, creating a legal SoC/ASIC custom package interface definition is not trivial. For a start, most important data signals have requirements preventing them from simply being assigned to any available pin/bump. Differential signals, as used in PCIe for example, often need to occupy adjacent pins/bumps to ensure phase control management and are often combined in pairs to form byte lanes. Memory busses, such as DDRx, introduce the need to manage signal skew across memory groups matched to an associated strobe clock.

Even a one-thousand signal pin custom package has so many possible interface assignment permutations that using static office spreadsheet programs render the task unsupportable beyond simply documenting a chosen assignment.

Obviously, the reality is that the space of all possible interface assignments contains both legal and illegal pin assignment definitions, as a number of package ball assignments may be fixed due to internal SoC/ASIC to package constraints such as hard IP blocks and IO assignments.

RISK ANALYSIS AND AVERSION

The risk introduced through leveraging SoC/ASIC-PCB interface flexibility is simple. If a single error exists in the interface, the resulting PCB will be non-operational. In worst case scenarios the SoC/ASIC-PCB interface error may cause catastrophic component damage (e.g., driving 20mA into a pin rated to accept 5mA). The costs associated with the interface errors greatly exceed any PCB manufacturing prototype costs. The real cost is to the design cycle time budget when weeks of expensive engineering time are consumed comparing PCB symbols and schematics to the SoC/ASIC package design to discover the exact error(s). This is a tedious and painful process that any experienced engineer will systematically avoid.

The natural and common design team reaction to the design complexity associated with SoC/ASIC – PCB interfaces and the need to maintain absolute synchronization of the Interface across design domain boundaries is to lock the SoC/ASIC-PCB interface design early in the design process.

If we were discussing a situation where we only had a couple dozen of pins comprising the SoC/ASIC-PCB interface, the interface error risk and signal complexity assignment would not be compelling drivers. However, we are dealing with devices that often have tens of thousands of signal pins.

DESIGN TEAM ORGANIZATION AND SILOS

To achieve PCB optimization, the SoC/ASIC package design team, the PCB functional design team, and the PCB physical design teams must all be in harmony. Many design organizations are moving/evolving toward the goal of having a "system" team comprised of chip/package and PCB functional engineers.

At the same time, primary business drivers have generated a chasm between functional design and physical design through outsourcing and "design anywhere, build anywhere" initiatives. At some point in the product design process, the electronic design is "thrown over the wall" from one team to another, creating organizational silos. Transcending the existing silos to achieve PCB optimization requires focused management effort to promote effective communication while minimizing design re-spin risk.

TRADITIONAL DESIGN PROCESSES

The dominant process for creating system PCB functional designs remains schematic based. The historic advantage of a schematic design process is the accurate communication of design intent through a symbolic representation. Schematic-based design methods have intrinsic costs and risks:

- Symbols for all components used in the design must be created and verified
  - Symbol interface errors result in non-operational PCBs
- Creating schematics and connecting the components is labor-intensive and time-consuming
  - Schematic errors result in non-operational PCBs

Creating a single symbol for a 1000+ pin SoC/ASIC device is labor-intensive, time-consuming, error-prone, and could result in the symbol not fitting physically onto a schematic sheet. To overcome the size issue, design teams will often create multiple (fractured) symbols for a single SoC/ASIC device increasing the labor, time, and validation investment.

Additionally, the value of the schematic to clearly convey design intent is obfuscated while maintaining the costs of the schematic design process.

At this level of detail, there is no mystery as to why design teams are reluctant to leverage the flexibility of SOC/ASIC interface design to optimize their PCB: the costs and risks associated with the symbol and schematic creation, maintenance, and validation process preclude "flexibility."

TIME TO MARKET CONSTRAINTS

Time to market is often a fundamental driver in the lack of interconnect integration planning between custom SoC/ASIC devices and their PCB designs. With the design development window under constant pressure to shrink, a key aspect of meeting time to market constraints is design risk mitigation.

As demonstrated by other barriers to PCB optimization, leveraging the flexibility of custom packages for PCB optimization is a key source of increasing design schedule risk. It is true that leveraging the flexibility of custom package interfaces has repeatedly proven to substantially reduce time to market. It is also true that this statement is only valid when advanced design technologies and methodologies are deployed to systematically address every PCB optimization barrier concurrently.

AVAILABILITY OF TOOLS

Typical custom package design tools today will automatically create a device/package specific legal signal-to-pin assignment. However, these solutions rarely consider anything but the SoC/ASIC in the creation of the interface; the PCB physical connectivity is almost never considered by the package design tools. And, to be fair, at that stage of the design process, the package interface assignments are usually already defined, and in most cases fixed.

Typically this interface planning takes place early, before the package design is completed, or even started, and the PCB is yet a distant task on a project plan. Once the design complexity is understood, the idea that the design optimization space can be adequately evaluated manually to achieve PCB optimization exceeds any reasonable expectation. This is where desktop office tools such as spreadsheets and their infamous bump/ball map usually come in.

The challenge with spreadsheets is that they are manual, error-prone, and use static data usually extracted from design tools, or worse, created manually. Spreadsheets cannot evaluate or communicate interface routing assignments or constraints to the upstream and downstream design teams. Nonetheless, spreadsheets have been used for many years to manage interface assignments between SoC/ASIC and the package balls. That being said, what about the following?

- Signal/power/ground (SPG) ratios and patterning to ensure quality return paths and power delivery

- Route paths for breakout escapes, layer assignments, and feasibility

- PCB-driven assignments, pin/interface compatibility for previous-generation designs

- Complex interface management (serial interfaces, memory, etc.) and their propagation across the substrates

BARRIER SUMMARY

It is the combination of risk assessment, historic and cultural processes and policies, required expertise, as well as the elemental interface complexity (the number of possible interface designs) that create the natural motivation to implement the Draconian practice of locking down the SoC/ASIC-PCB interface early in the design process, often without much thought or care for its impact on downstream design. It is the unjust harshness of locking the SoC/ASIC-PCB interface early that precludes PCB optimization and puts your product profit margin outside the value-add of the typical engineering design process.

THE POTENTIAL EXISTS

Capitalizing on SoC/ASIC adoption and leveraging the power of custom package interface flexibility has allowed early adopters of PCB centric optimization to experience impressive results:

- Eliminating a minimum of one person-week per 500 SoC/ASIC pins on the system PCB design.

- Reducing trace length by 25% to 50% and enjoying a corresponding performance increase

- Eliminating up to 150 PCB vias for every 500 SoC/ASIC pins

- Reductions in interface design times as much as 60%

- Transforming previously un-routable PCBs into routable PCBs using the same PCB layer stackup

- Total design cycle reduction by as much as 50%

In a competitive landscape where fighting for a reduction of PCB manufacturing cost advantage and a day of time to market acceleration could define the difference between windfall profits and a "boat anchor" there are not many opportunities to realize a 50% design time to market advantage.

THE POWER OF THE TSUNAMI

Cleary, taking advantage of the flexibility of SoC/ASIC devices and their custom Package to optimize PCB design for product profit margin is a critical evolution of standard system PCB design processes. The truth is that this level of PCB optimization represents the first plateau in PCB optimization opportunities.

Customers entrenched in their corporate infrastructure, processes and policies often confront PCB optimization for the first time when they attempt more complex system PCB designs containing a new custom SoC/ASIC device. A common reaction is to attempt re-architecting the system design to reduce complexity or increase the number of routing layers on the PCB...anything but confronting the barriers and opportunities associated with PCB optimization.

Applying PCB driven SoC/ASIC optimization represents the next plateau of PCB optimization. Are you aware that SoC/ASIC custom package flexibility could be used to eliminate additional routing layers from your PCB? Most design teams are trapped in the "time-to-market" crunch and never have the opportunity to research this level of PCB optimization let alone develop the necessary technical skills and deploy the methodologies that are available.

The doorway to PCB optimization has been opened but the final destination has no road markers. The power, size, and complexity of SoC/ASICs continue to evolve, as does the custom IC Package that integrates them with the system PCB. The survival question to ask yourself is: Are you on the right PCB optimization path for success?

THE RIGHT TOOLS EXIST TODAY

Mentor Graphics, a Siemens Business, developed Xpedition® Substrate Integrator in partnership with some of the world's largest and most influential semiconductor and systems companies. The unique flow results in substantial costs savings for electronic component/device and system PCB developers and its lightweight, graphical, canvas-based environment enables fast, multi-substrate, what-if rapid prototyping with concurrent interconnect optimization across SoC/ASIC, package, and PCBs.

Xpedition Substrate Integrator can radically increase design productivity and overall device performance while optimizing logical connectivity that can reduce PCB layer count, interconnects, and via usage. Its PCB-driven package-optimization process uses a current or reference PCB design to optimize critical signal performance and enable optimization of the PCB/package interfaces.

The combination of technology leadership and strong partner-customers supported the development and validation of PCB optimization, turning it into a key competitive advantage for system PCB design teams.

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