IMPLEMENTING HIGH-DENSITY ADVANCED PACKAGING (HDAP) FOR OSATS AND FOUNDRIES

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Moore's law is increasingly difficult to maintain and is driving growth of innovative packaging technologies in response to system scaling demands. These innovations are increasingly in the form of fan-out wafer level packaging (FOWLP) or multi-substrate / multi-device packages like interposers and system-in-package (SiP).

New challenges come with these disruptive technologies as they employ silicon-like features and processes or multi-substrate architectures to facilitate high-performance memory devices like HBM/HMC.

Today's package design methodologies and tools are at an inflection point as significant as the transition from MCAD tools for lead frames to ECAD tools for PBGAs. The entry of silicon foundries into the packaging supply chain further disrupts tools and methodologies with their application of silicon PDKs (Process Design Kits) and verification processes to packaging.

THE MOVE TO HDAP

At Mentor we coined the term 'HDAP' (High Density Advanced Packaging) to categorize the disruptive packaging technologies that present unique challenges to traditional design tools and methodologies (Figure 1).

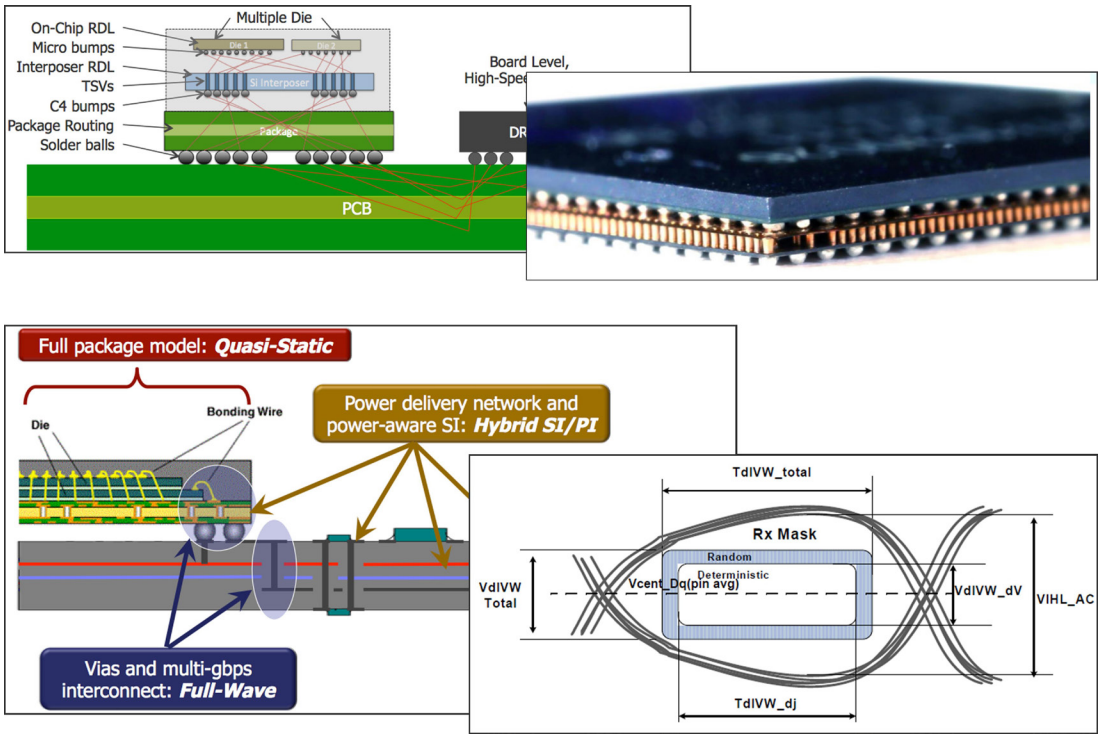


Figure 1: HDAP can be characterized by multi-substrate / multi-device packages that require device / substrate stacking using high pin count devices / designs.

The most well-known and publicized form of HDAP is the fan-out wafer-level packaging (FOWLP) that is rapidly gaining popularity in the fabless semiconductor market. FOWLP was given broad public attention through TSMC and their InFO FOWLP process and Apple®, whose iPhone® 7's ASP has packages using InFO. However, there are also many other suppliers offering proven FOWLP processes. Here are a few of these well-known suppliers:

- Amkor/NANIUM - SWIFT (chip last version), 300mm wafer eWLB
- ASE - FOCoS, also "chip last" panel version based on Deca M-Series
- NEPES - 300mm line in Korea with RCP process
- Powertech Technology - 300mm line, panel development
- SPIL - 300mm wafer, eWLB-like
- STATS ChipPAC - 300mm wafer eWLB

With the recent explosive growth of FOWLP, there is increasing use of 'IC-like' process and tools which necessitates a higher data resolution and DRC accuracy for smaller feature sizes. GDSII quality and performance on non-Manhattan geometries can also be an issue for traditional packaging tools.

I/O counts on ASICs, FPGAs, and SoCs can approach or surpass 10K pins which can easily impact design tool performance, capacity, and throughput.

Although FOWLP is the most common HDAP technology that's in broad deployment today, it's not the only HDAP technology that exists and is production proven. The other common HDAP package types are 2.5D using silicon interposers, Chip-On-Wafer-On-Silicon (CoWoS), and Wafer-On-Wafer (WoW).

HDAP can be thought of as a new technology 'node point' that requires a substantially different design flow, similar to how the organic laminate BGA substrate was a 'node point' evolution from its lead-frame predecessor that gave rise to new design flows, tools, and processes.

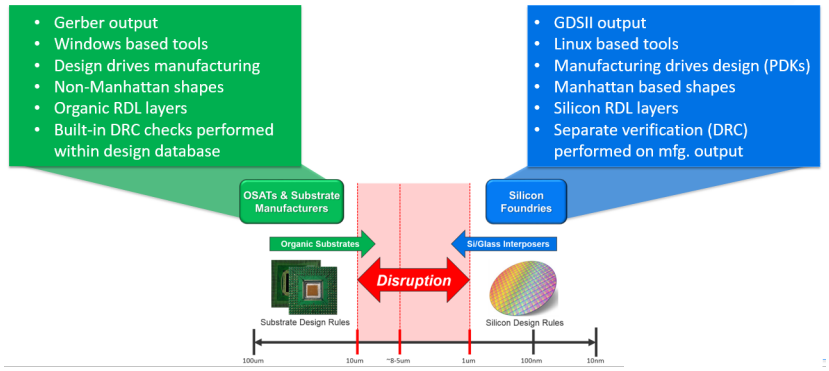


Figure 2: Some of the major differences between traditional PBGA packages and the new HDAP packages.

Differences between today's well-understood PBGA flow and HDAP (Figure 2) are common across all types of HDAP and present some unique challenge to existing design tools, methodologies, and processes. Examples include:

- Prototyping of multi-die integration and optimization (critical for interposer-based designs)
- Connectivity planning and coordination of high-performance interfaces across substrate boundaries
- Device and substrate stacking – 3D interoperability
- Shrinking feature sizes and new geometries
- Place & route support for TSV, micro-bumps, silicon interposer redistribution layer (RDL), and signal routing
- Increasing pin counts on devices and overall design
- Assembly-level verification (LVS & LVL) of individual design substrates and complete assembly
- Mask-level fabrication verification of individual substrates
- Electrical extraction and analysis of the completed assembly

THE IMPORTANCE OF PROTOTYPING

Different types of HDAP are generally best suited to different end-application markets and different applications. FOWLP is frequently considered a better fit for automotive, radio frequency (RF), and mobile products, whereas 2.5D designs with silicon interposers are best suited for memory, FPGA, and APU/GPU/CPU applications. However, irrespective of the type of HDAP, they all benefit from prototyping prior to detailed implementation.

Prototyping enables the design engineer and/or project architects to evaluate die locations (x, y, & z), explore interposer options (if applicable), build system-level assembly netlists (from die-source Verilog, import of external connectivity (csv), or directly), and evaluate critical interface assignments and implementation viability. Prototyping before detailed physical design has been proven to reduce ECOs and provide greater predictability to the design process.

Prior to HDAP, prototyping was usually done non-graphically, with spreadsheets, often known as 'bump-ball' maps. This was more of a documentation process than prototyping as spreadsheets cannot give the engineer 'what-if' views or manage ECO changes in connectivity or assignments.

HDAP prototyping, especially in a graphical environment where all design elements can be visualized and interacted with, provides an optimal end solution without costly project delays or iterations caused by late identification of issues. Investing in cross-substrate prototyping and planning during the early stages of design can greatly improve predictability during implementation by finding and fixing cross-substrate issues before they become late-stage surprises. An early-system perspective with cross-substrate visibility improves communication and coordination by providing immediate feedback on decisions that are typically made on an individual substrate basis.

A simple example would be optimizing package substrate ball pad assignments solely in the context of the die that creates an overly complex PCB net list – resulting in extra trace length, vias, or, worse, layers (cost) at the board level.

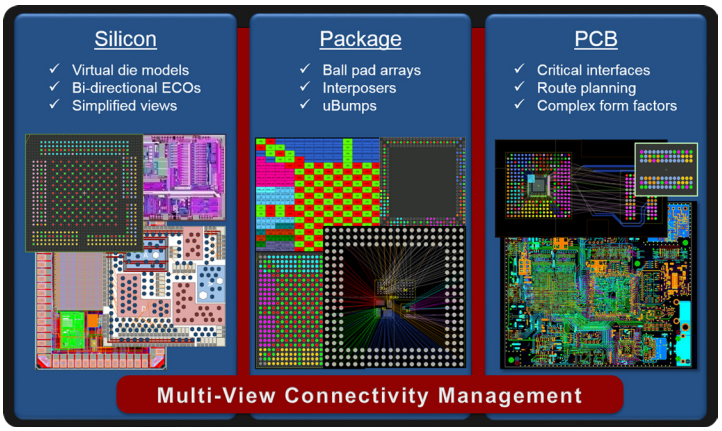


Figure 3: Visual prototyping using abstracts of the complete HDAP design, including target PCB (if applicable), provides the engineer/architect with a sandbox canvas to explore options and design viability.

Other benefits of HDAP prototyping include:

- Quick evaluation and convergence on the best, most cost-effective configuration(s) from a system perspective
- Reduced tendency of working in a vacuum which can result in over-design or needless complexity
- Better management of cross-substrate transitions

The macro goals of HDAP prototyping can be summarized as:

- Construction, coordination, and management of multiple substrates in one environment
- Development/creation, planning, management, and visualization of system connectivity across IC-Package-PCB
- Supporting substrate-specific land patterns for a single device including compensation
- Generation and synchronization of library data for use during PCB design
- Targeting of multiple packages or PCBs (if needed)

Once the prototyping phase has yielded a feasible and acceptable design scenario, it's time to move into detailed design implementation.

HDAP DESIGN

HDAP design presents its own set of unique design and verification challenges. Historically, package design and IC design have been isolated processes, with little in common. Bringing them together requires melding the two into a single cohesive flow.

ICs are designed primarily in a Linux® operating environment, using electronic design automation (EDA) tools certified by a target foundry or fab and associated with a specific PDK. System-on-chip (SoC) designs are typically built using Manhattan geometries represented in gridded formats like GDSII or OASIS. When the IC design is sign-off ready, the final approved design files (tapeout) are sent to the foundry for manufacture. When finalized, a die abstract (indicating the die's size and the individual pin locations) is passed to a package design team using any one of several formats (LEF, AIF, etc.).

The package design community predominantly works with EDA tools designed to run on a Microsoft® Windows® operating system. Packaging design uses non-Manhattan geometries extensively, and does not often map nicely to the gridded formats of the IC world. In fact, the two worlds share very few standards in terms of data representation. Package designs, along with the physical die, are historically transferred to a package house or OSAT facility using a number of formats, such as AIF, ODB++, and even Gerber. Typically, there is very little in the form of formal sign-off requirements that accompany the package design other than a textual document describing the intended design rules.

Surprisingly, even though very few common standards exist between these communities, no new standards are needed to bring the two together. It turns out that data-format conversion in combination with tool-to-tool interfaces and communication protocols can be used to meet the needs of all the parties involved. While communicating between Microsoft Windows and Linux can be tricky, experience has shown it can be achieved readily and pragmatically using a virtual network connection (VNC).

HDAP IMPLEMENTATION

Implementing a unified HDAP design approach requires a significant expansion in communication between the IC and the package design worlds. For instance, if you want to optimize the package design for size and/or performance, then you must optimize the entire system, not just the individual elements. An IC designer might be able to design a really small IC but, in doing so, it might be more difficult to connect that die into the package, thus expanding the package footprint. Similarly, a package designer might be able to design a clean and tight package, while making it impossible for the IC designers to get their die I/Os to match specific locations. To optimize the entire package design, IC designers must know more about the intended package, and package designers must know more about the ICs included in the package.

There are also a number of technical challenges that must be managed, ideally by the design tools. Some of these issues include:

- Silicon RDL layers, organic RDL layers, or mold/plastic layers. Each type has its own unique design rules to increase yield.
- Stress relief. Minimizing straight lines helps, but makes verification more challenging.
- Copper areas require complex outgassing perforations to prevent substrate warping and copper density balancing across the design.
- The connection path from die pad to copper conductor path requires filleting, the addition of metal to smooth the transition between geometry dimensions.
- Potential die shift during assembly requires flexible, adaptive patterns.
- Producing clean fab-ready GDS.

HDAP PACKAGE DESIGN

Mentor's Xpedition® Substrate Integrator technology helps IC, packaging, and printed circuit board (PCB) co-design teams visualize and optimize complex single or multi-chip packages integrating silicon-on-board platforms. The Xpedition Substrate Integrator co-design methodology automates the planning, optimization and connectivity from a chip through multiple packaging variables.

In the HDAP environment, Xpedition Substrate Integrator and Xpedition Package Designer provide the integration/co-design platform for IC, board, and package that supports PCB, multi-chip module (MCM), system-in-package (SiP), RF, fan-out, and BGA designs. This flexible, multi-mode design platform provides a single, hierarchical view of the system that is easy to extend through the Microsoft component object model (MS COM) and industry-leading routing technology. Xpedition users can drive rule-based I/O-level optimization and perform pin and ball-out

studies from their respective domains, visualizing the impact across the complete system, and generating an automated central data library in the process.

Cross-domain capabilities in Xpedition include:

- Connectivity management
- Design-domain connectivity models
  - Hardware description language (HDL), table/spreadsheet-based and schematic editing modes
- Cross-domain signal shorting and splitting with automatic pin-mapping
- System-level connectivity tracking and verification (source netlist)
- Design tool aggregation
- Interconnect optimization focused on layer reduction and improved signal quality
  - Visualize and optimize interconnect across system
  - ICs, interposers, packages, and PCBs
  - Smart unraveling of interconnect paths

A common problem with conventional package-design tools and methodologies is that the design will pass DRC within the layout tool but fail once the outputs are checked with manufacturing physical verification tools (Figure 4). This can be due to a number of factors:

- Area-fill algorithms
- Lack of arc constructs
- Quality of GDS output
- Polygon merge
- Accuracy or resolution in host design tool

A related problem often seen is the insertion or substitution of shapes into the output files due to lack of support within the layout tool – mesh pads, graduated degassing etc. Such HDAP common entities must be handled directly within the design tool, otherwise their absence creates a discontinuity between the layout database and what's actually manufactured (Figures 5 and 6). Major examples of the discontinuity caused by an out-of sync layout database and GDS are:

- Data synchronization – impact of ECOs
- Accuracy of electrical analysis – typically run off layout DB.

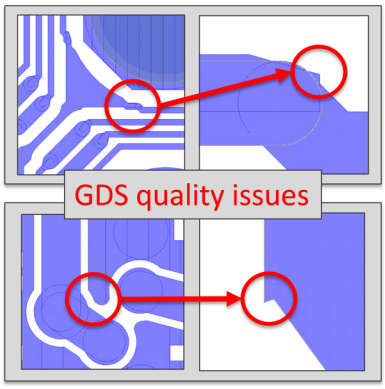


Figure 4: Typical design-related GDS quality issues found using traditional package-design tools

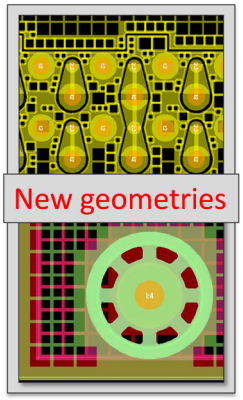


Figure 5: HDAP introduces many new manufacturing process-related geometries that should/must be managed within the package design tools.

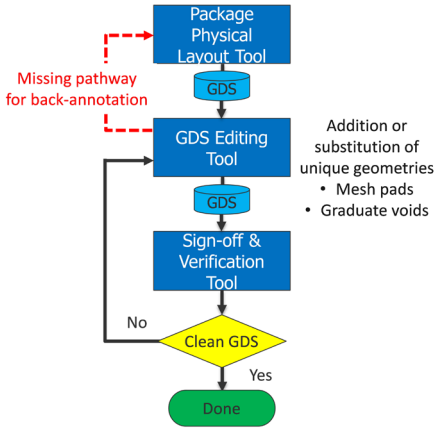


Figure 6: Here we see a common problem with traditional packaging tools that rely on post design GDS editing.

HDAP PACKAGE LAYOUT

Xpedition Package Designer provides a comprehensive, focused solution for HDAP layout through to mask-ready manufacturing output. It delivers ease-of-use with advanced functionality providing designers the technology to create today's complex single or multi-die packages. Powerful die-attach capabilities provide support for wire bond, flip-chip, stacked die, System-In-Package (SiP), and Package-On-Package through to the latest wafer-based methodologies such as FOWLP and CoWoS. It's designed specifically for HDAP and provides the following important

HDAP design capabilities:

- Comprehensive die and BGA import/creation utilities
- Fast on-the-fly connectivity creation (Layout Driven Design)
- Auto-assisted sketch routing that delivers the industry's highest routing productivity
- Integrated 2D-3D editing and visualization
- Powerful, fast, and accurate, dynamic metal area fill with parameterized mesh and degassing holes
- Embedded HyperLynx® 3D quasi-static field solver for package model creation
- Embedded HyperLynx DRC custom-rule engine for in-design ECOs that reduce the potential for manufacturing mask signoff-driven ECOs
- Fast predictable path to GDS verification and signoff
- Direct integration with Calibre® for identification and resolution of DRC issues

With many HDAP package types employing 2.5D or even 3D for integration of substrates, the need to visualize and even design in 3D is becoming a necessity. 3D not only helps the designer understand what they are creating but it can greatly reduce errors and increase productivity by providing ways to visualize and interact with the design beyond the typical 2D (Figure 7).

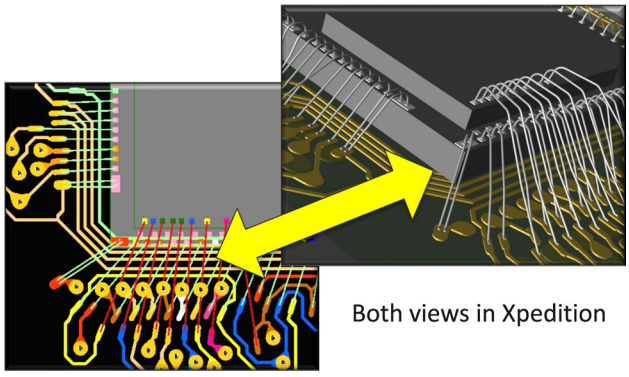


Figure 7: Xpedition Package Designer provides real-time 2D & 3D design viewing and editing.

ACHIEVING FABRICATION-READY GDS

For HDAP to become a repeatable, predictable design process, the design tools involved must be capable of producing fabrication-clean GDS or, at minimum, be capable of taking back GDS corrections identified and addressed during sign-off verification (Figure 8).

Once the design has passed fabrication signoff, it needs to be verified for assembly.

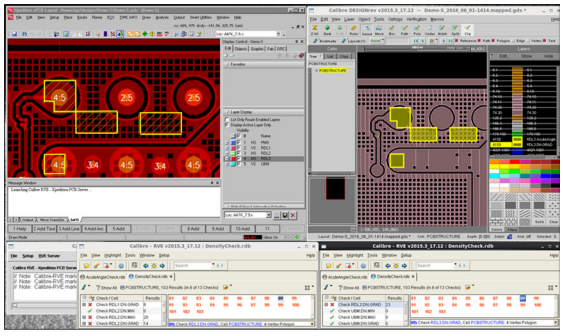


Figure 8: Xpedition Package Designer and Calibre are directly integrated, even across Windows and Linux platforms

HDAP VERIFICATION

HDAP package designs require both physical and logical assembly verification and validation. The die must correctly align with its corresponding landing pads on the interposer or package substrate (LVL). The checks required are alignment, pad size, and pitch scaling and pad-to-pad overlaps. On the logical side (LVS), you need to ensure that connectivity actually exists between connected objects/shapes, verify the location of electrical pins, and check for mismatched connections (Figure 9).

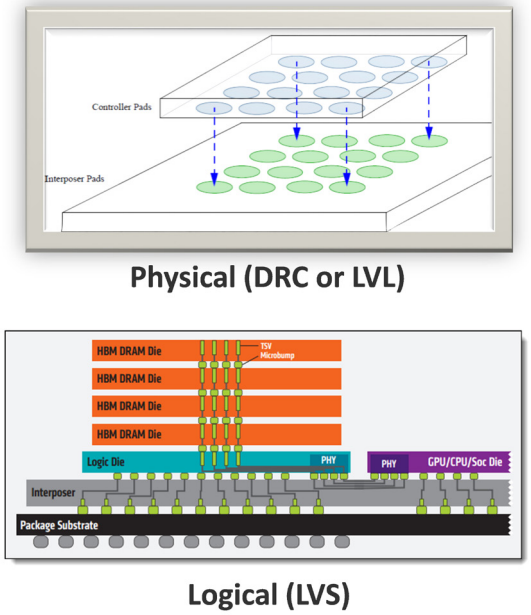


Figure 9: Primary checks for HDAP applications

While this sounds very challenging and complex, it's not impossible. We can significantly simplify this process when we realize that it's not necessary to check every geometry in every die. Each individual die already will have been checked for its target foundry with respect to DRC and LVS. All we really need to do is check the interactions between the dies. That is not to say this is trivial. In some cases, this can require extracting several layers within each die to see what their impacts are. In either case, it does require that the tool understand the layering per die and per placement.

The typical process is as follows:

- Verify individual components stand-alone
  - Maintain standard DRC, LVS, PEX processes
  - Check per process requirements
- Define and check 3D assembly interfaces
  - Consider: offset, rotation, scaling, etc.
  - Verify die, pad, bump, and ball placements
  - Trace connectivity through assembly stack-up
- DRC and LVS
  - Check package connectivity to die pins
  - Check physical geometric relationships and overlaps

Most checks, or design rules and design parameters, will be defined by the foundry or OSAT as they directly impact their manufacturing process and ability to achieve yield goals. With HDAP being a part-silicon, part-package design process, the foundries have a proven process and methodology to define, share, and drive design, verification, and signoff with their IC design customers. It's known as a PDK (Process Design Kit) and associated DRM (Design Rule Manual).

IC designers use these PDKs not only to reduce their risk but also to improve overall productivity by implementing repeatable, proven verification techniques.

Until now, chip design companies and OSATs have had no corresponding signoff verification process to ensure that an IC package meets manufacturability and performance requirements. This lack of qualified verification processes puts package designers at a significant disadvantage compared to their IC design counterparts.

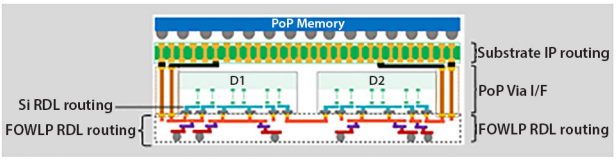
Package die are often produced using multiple processes and multiple foundries. This not only raises the level of complexity, it also exposes the need for a process to ensure that these disparate products can be manufactured within a single package. Package designers must often work with poorly documented and/or inconsistent processes each time they submit a package design. In addition, the new class of packages now coming into the market enhances the interactions between the layers, so there is no clear separation between the traditional die and package.

The challenges of verifying IC packages are numerous. Die design teams often have very different goals from the package design team, which creates unforeseen integration issues. Chips often come from different foundries and are verified using different processes, making package failures hard to identify and fix. There hasn't even been a formal verification process to ensure that the connectivity from a single die to the package's BGA is correct. We simply haven't had good characterization of package processes and requirements, leaving chip designers and OSATs to muddle through on their own.

Not that the industry isn't trying. OSATs have built and manufactured packages for years, and developed a variety of tools to help in the process. However, each design team must write its own rules for each assembly, with no reference signoff deck to ensure the manufacturability and performance of the package. In addition, OSATs rarely hold their customers to a hard and fast rule deck like a foundry does.

What is beginning to emerge as part of the HDAP design process is a new approach for fabrication sign-off and physical verification of HDAP designs, something called an assembly design kit (ADK). The purpose of an ADK is similar to that of the PDK—to ensure manufacturability and performance. What makes that happen, in both PDKs and ADKs, are things like standardized rules that ensure consistency across a process, qualified tool flows, interface formats, and input/output formats—in short, everything a designer needs for successful design, tested and qualified and proven to produce working products. For example, one component of an ADK would be sign-off checks for the package layers and interacting die layers, without reference to any kind of layer mapping.

Assembly design kits will provide many benefits to the industry: reduced risk of package failure, increased packaging business, and increased use of 2.5/3D packages. And we have already seen the successful use of a conceptual ADK using the first basic building block of Calibre 3DSTACK (Figure 10). In this case, a 3DSTACK deck has been created and qualified by Stats ChipPAC, a leading OSAT using their eWLP wafer-level process. This rule file has been adopted and proven in production at Qualcomm on an assembly comprising two die connected through the package RDL. The rules from Stats ChipPAC include the DRC rules for the package layers themselves plus checks to ensure that the dies are interacting and connecting within the package properly.



Implementation Details

Verify DRC & LVS across I/F boundaries
- Between package and dies

DRC checks on RDL layers
- Avoid orthogonal/90° angles on RDL geometries
- Area-dependent line width & spacing (L/S) checks

Metal density checks
- Fill check for floating metal fill pattern and/or biased metal plane with slotting
- Local-based density checking

Assembly rule checks
- Die-to-die edge
- Die-to-package edge
- Die-to-package alignment
- Corner rules
- Landslide Caps to BGA spacing

Mechanical stress checks
- Die-package Fan-out ratio

Figure 10: Example of an ADK-driven HDAP project between Qualcomm and STATS ChipPAC

The OSAT or foundry determines the connectivity stack for LVS comparisons on HDAP designs and creates design rules to address package-specific and die-to-package geometric interface requirements (Figure 11).

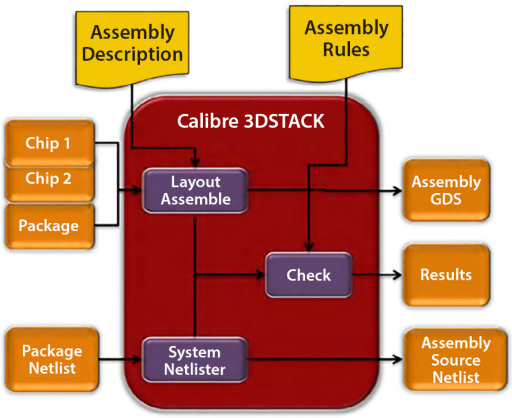


Figure 11: The Calibre 3DSTACK functionality enables and supports all the unique verification and signoff needs of HDAP designs and is directly integrated with the Xpedition HDAP design tools.

SUMMARY

The requirements and challenges of HDAP design and verification demand new EDA tools, functionalities, and flows. HDAP design and verification require cooperation and collaboration between design houses, OSATs, foundries, and EDA vendors. With common tools that have the integration and functionality needed to operate in both the IC and packaging domains, companies can reduce turnaround time and the risk of package failure. Mentor's Xpedition HDAP flow ensures that package designers, foundries, and OSATs have all the design and verification capabilities needed to take advantage of this exciting HDAP packaging technology and the markets it serves.

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