SOLVING THE DESIGN AND VERIFICATION CHALLENGES OF HIGH DENSITY ADVANCED PACKAGING

KEVIN RINEBOLD AND KEITH FELTON, MENTOR GRAPHICS

WHITEPAPER

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INTRODUCTION / SUMMARY

Today's electronic products present new challenges to product development teams. As a result, there is a constant push to improve product quality and design efficiency through the use of new design technologies. For example, system-scaling demands change as Moore's law becomes increasingly difficult to maintain, thus driving growth of innovative PCB and packaging technologies such as:

- High-density interconnect and rigid-flex to enable more functions per unit area
- Advanced packaging such as System-in-Package (SiP) and Fan-out Wafer Level Packaging (FOWLP) to enable the steady increase in design density (Figure 1).

These innovative 2.5D and 3D "high-density" advanced packaging (HDAP) solutions not only disrupt traditional design methodologies and tools, they also disrupt the supply chain. With these disruptive technologies come new challenges as they employ silicon-like features and processes, or multi-substrate architectures to facilitate high-performance memory devices like High Bandwidth Memory and Hybrid Memory Cube HBM/HMC.

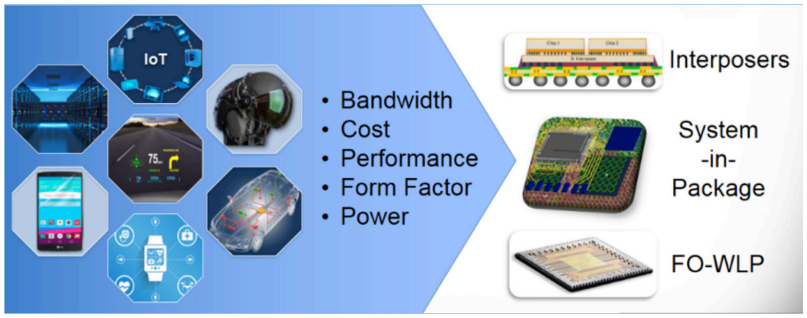

Figure 1: Industry demands are driving innovative packaging solutions

Package design methodologies and tools are, in fact, at an inflection point, one that is as significant as the transition from MCAD tools for lead frames to ECAD tools for Plastic Ball Grid Arrays (PBGAs). The entry of silicon foundries into the packaging supply chain further disrupts tools and methodologies with their application of silicon process design kits (PDKs) and verification processes to packaging. To draw an analogy to the IC world, these 2.5D and 3D HDAP technologies are in fact new "nodes" for packaging and as such require a new design and verification methodology.

BACKGROUND / PROBLEMS

Today's well-understood processes for organic substrate packaging are very similar to those used for PCB design. The design rules provided by the substrate fabricator are of a fairly simple nature and usually allow for some freedom for flexibility. This PCB-like process is used by the outsourced assembly and test (OSAT) for today's PBGA package which uses organic substrates, typical FR4, or polyimide. These basic, flexible rules rarely differ across OSATs, giving the designer a level of supplier flexibility without excessive design retargeting.

Compare that with the complexity of fabrication rules that are specific to the silicon foundry which are driven by process and yield. In this case, the fabrication rules are usually not flexible and cannot be shared or interchanged across different foundries. 2.5D/3D high-density

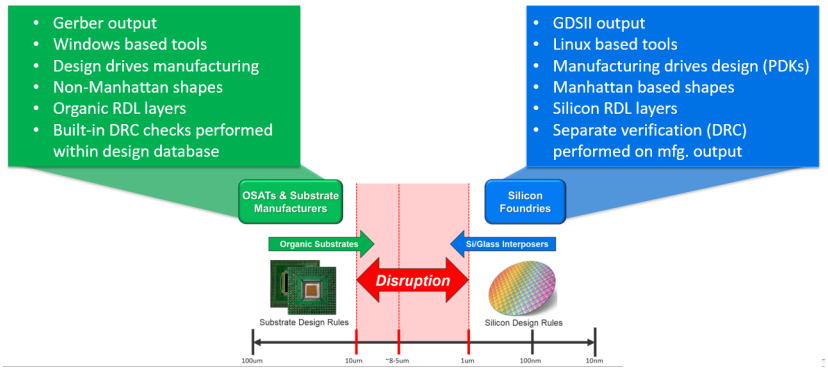

Figure 2: 2.5D/3D technologies are part silicon and part package

advanced packaging technologies are part silicon and part package with different design methodologies and characteristics (Figure 2).

The term "high-density" advanced packaging (HDAP) refers to the category of disruptive packaging technologies that includes: FOWLP, interposer-based packages, high pin-count flip chip, and SiP.

A common theme across these packages is that they all present some unique challenge to traditional design tools and verification methodologies. Many of today's packages incorporate some element of multiple substrates or multiple devices to deliver solutions for system scaling.

The design and verification challenges include:

- Connectivity planning and coordination of high-performance interfaces across substrate boundaries
- Device and substrate stacking – 3D interoperability
- Electrical extraction and analysis of the completed assembly
- Mask-level verification of individual substrate and completed assembly.

With the explosive growth of advanced packages like FOWLP, there is increasing use of "IC" like process and tools which necessitates higher data resolution and design rule check (DRC) accuracy for smaller feature sizes. GDSII quality and performance on non-Manhattan geometries can also be an issue for traditional packaging tools. Furthermore, the I/O counts on ASICs, FPGAs, and System on Chip (SoC) devices may approach or surpass 10K pins. As such, they can easily impact design tool performance, capacity, and throughput.

High-density advanced packaging characteristics are not addressed by packaging design tools that focus on plastic ball grid arrays. A PBGA-focused tool that is "stretched" for a HDAP design will introduce errors and force time-consuming iterations downstream before tape-out. For example, if a FOWLP design is to utilize multiple substrates (interposers) and/or devices, new design capabilities will be required in order to accurately construct and verify the package.

Verification of HDAP, including FOWLP, brings a new set of challenges to the package designer and the product development team. The verification and sign-off process when using the aforementioned IC like processes is new, and very different to the usual path and process for PBGA designs.

One of the most common problems when using conventional package methodologies for HDAP is that the design will pass DRC within the layout tool but fail once the outputs are checked with the manufacturing physical verification tool. This can be due to a number of factors:

- Weak area-fill algorithms
- Lack of arc constructs
- Quality of GDS output
- Polygon merge
- Accuracy or resolution in design tool

Attempting to resolve this problem leads, in turn, to issues associated with the need to insert or substitute shapes into the output files due to lack of support within the layout tool. This "work-around flow" naturally creates a discontinuity between the layout database and what is actually manufactured (Figure 3).

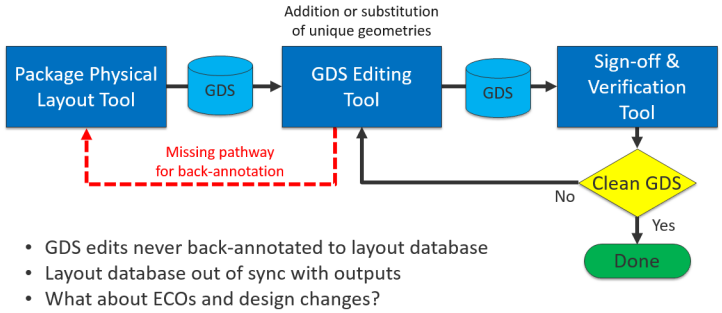

Figure 3: Work-around flow when using conventional package methodologies for HDAP

SOLUTION

As previously stated, the challenge for product development teams is how to apply silicon (IC) type processes to the design and verification of 2.5D and 3D packages. To address this challenge, Mentor Graphics developed an innovative design and verification solution that directly addresses the common, yet challenging, design and verification requirements of HDAP, FOWLP, and SiP and derivative processes such as TSMC's integrated fanout (InFO).

Fully certified by TSMC® for both InFO_M and InFO_POP packaging technology, a key component of Mentor Graphics' HDAP solution is substrate integration, the planning and optimization of logical connectivity between the multiple substrates prior to detailed physical implementation. See Figure 4.

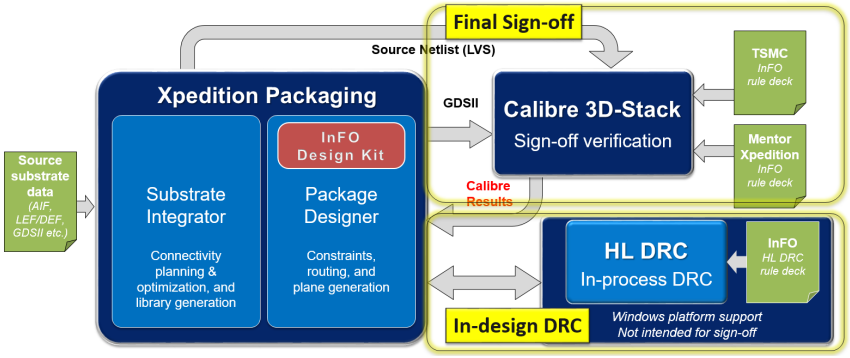

Figure 4: Mentor Graphics' TSMC-certified InFO design and verification flow

In the Xpedition flow, Substrate Integrator provides early, fast, and efficient multi-substrate integration and design management. Substrate Integrator is exceptionally flexible, accepting various input formats such as LEF/DEF, AIF, GDSII, and others. This flexibility allows system netlist generation and tracking, thereby eliminating the need for management of connectivity and device information through spreadsheets and simplifying and accelerating the overall ECO process.

Substrate Integrator also provides the designer with the complete picture: die, interposer, package, and PCB in one graphical environment. This allows the design team to:

- Better anticipate and avoid downstream issues
- Efficiently perform and evaluate trade-offs and design scenarios with the ability to clearly communicate decisions to stakeholders
- Achieve the right balance of connectivity and assignments for optimal performance, cost, and manufacturability prior to implementation— resulting in fewer iterations and shorter cycle times.

HDAP designs often involve complex fabrication/foundry rules regarding allowable metal structure geometries. Designing and verifying metal structures using a signoff process can be time-consuming, especially for multiple iterations.

Another component of the Xpedition HDAP solution is the use of HyperLynx® technology to quickly identify and resolve substrate-level DRC violations with in-design checking. This approach typically addresses 80-90% of problems prior to final tape-out sign-off verification. It also provides independent verification, separate from the design tool's DRC engine, for greater confidence in result accuracy.

Physical verification of 2.5D/3D packages requires a method for treating each placement layer uniquely without overwhelming tool capacity and performance. Given that multiple placements of a single die are possible, accurate checks of these systems require each layer to be differentiated per die placement.

Fortunately, this is a manageable task as not every geometry in every die needs to be checked individually. Because each die already will have been checked with respect to DRC and layout versus schematic (LVS) for its target foundry, all that remains is to check the interactions between the dies. In some cases this can require extracting several layers within each die to determine their impacts. As such, there is a requirement that the design tool understand the layering per die and per placement. In the Xpedition HDAP solution, Calibre® 3DSTACK technology provides multi-die and interposer LVS checking, resulting in fast, accurate results. Xpedition's integration with Calibre also ensures a very robust sign-off path for HDAP designs.

CONCLUSION

Headlines like "iPhone 7 Adopts Fan-out Wafer Level Packaging Instead of PCB" and "Samsung's new FOWLP tech doesn't need a PCB" are indicative of just how critical high-density advanced packaging is to today's leading-edge electronic designs. Mentor Graphics' innovative HDAP design and verification solution addresses the unique requirements associated with these disruptive technologies.

The Xpedition solution ensures that 2.5D/3D detailed implementation is achieved in an environment that includes extensive design capabilities such as native 3D design visualization, editing, and 3D DRC. It utilizes in-design verification to address 80-90% of problems prior to final sign-off. Furthermore, the solution is a closed-loop flow to ensure data synchronization between outputs and the final layout database. Direct, proven integration with Calibre 3DSTACK provides uncompromised signoff and LVS verification.

For the latest product information, call us or visit: www.mentor.com

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Trust Tower
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

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