Amkor’s SLIM & SWIFT Package Technology

Ron Huemoeller | SVP Advanced Package Technology Develop & IP
Amkor’s Package Technology Integration Roadmap

Substrate Level
(On Board RDL)

Wafer Level
(Bump Line RDL)

Foundry Level
(BEOL Damascene)

Mobile Products
(SiP, fcCSP, PoP, Wfr Level)

High Perform Products
(SiP, FCBGA)

- • SWIFT: Silicon Wafer Integrated Fan-out Tech
- • SLIM: Silicon-less Integrated Module

- FCBGA
- Adv Subst Process
  (dual substrate)
  (Multi die)
- Thin Film on Subst
  (Multi die)
- Si Interposer
  (Multi die)
- SLIM
  (Multi die)
- Advanced Fan-out WLP
  SWIFT™
  (Multi die)
- 5um L/S
- 10um L/S
- 2um L/S
- HVM
- LVM
- Proto
- Develop
- fcCSP
- WLCSP
- Fan Out WLP
  (Single/Multi die)
SLIM & SWIFT Package Definition

SLIM™
Silicon-Less Integrated Module

SWIFT™
Silicon Wafer Integrated Fan-out Technology

- Top die
- U-bump solder joint
- Fab. BEOL layer
- RDL layer
- BGA
Amkor’s Advanced Wafer Product Positioning

- **Multi dies, SoC partition, 3D compatible**
- **< 2um L/S by foundry interposer BEOL**
- **High performance (CPU/GPU), mobile AP, BB**

**W-SLIM**

- **Multi die, SoC partition, HBM, 3D compatible**
- **RDL 2~10um by bumping line; Mobile AP/BB**

**SWIFT**

- **Single or Multi die integration**
- **RDL 6~12um by bump line; RFIC & PMIC**

**Fan-Out**

- **Single die**
- **RDL ≥ 10um by bump line**
- **RF, WLAN, Power etc**

**WLCSP**

Products: RF and Analog to Advanced Processors

Performance
Amkor’s Advanced Flip Chip Product Positioning

- **S-SLIM**
  - Multi die, SoC partition, HBM, 3D compatible
  - RDL ≤ 2um L/S by foundry BEOL interposer
  - Ultra Thin
  - Lower cost ; SLIM < 2.1D < 2.5D

- **2.5D**
  - Multi die, SoC partition, HBM, 3D compatible
  - RDL ≤ 2um L/S by foundry BEOL interp. + TSV
  - HBM integration
  - RDL 2~10um L/S by substrate

- **2.1D**
  - Single or multi die
  - RDL > 10um L/S by substrate
  - 3D compatible

Products : AP, BB, CPU, GPU and Networking
SLIM Platform Technology
Amkor’s Advanced Flip Chip Package Platform
SLIM™: Value Proposition

- **Lower Cost**
  - Simplified wafer construction
  - Simplified wafer processing

- **Supply Chain Flexibility**
  - No longer tied to TSV formation

- **Reduction in Package Thickness**
  - Simplified wafer construction
  - Elimination of wafer back-side process steps compared to 2.5D

- **Leverages 2.5D wafer processing and assembly equipment and expertise**
SLIM™: Amkor’s Most Advanced Packaging Solution
Silicon-Less Integrated Module (SLIM)

- Foundry BEOL layers retained
- Same CuP bond pads
- Same UBM and solder bump
- No TSV
- Much thinner

2.5D TSV Si Interposer

SLIM™
(non-TSV interposer)
SLIM™ // 2.5D Construction Comparison

2.5D

SLIM™

Top Die
Cu-Pillar Bumps
TSV
C4
BEOL Layer
M1 Contact

μ-bump pitch
SLIM: Process Simplification

**MEOL Process**

1. **Wafer Thinning**  
   - simplified
2. **Si recess (Dry Etch)**  
   - simplified
3. **SiO2 Opening (Dry Etch)**
4. **UBM + Bump or BGA**
5. **TSV Reveal (CMP)**

**2.5D TSV Interposer Silicon**

- **1. Wafer Thinning**
- **2. Si recess (Dry Etch)**
- **3. Passivation (PECVD)**
- **4. TSV Reveal (CMP)**
- **5. UBM + Bump**

**Wafer-level SLIM™ 2 Die 3D**

**Front Side Bump**

**Top Die Attach on Interposer**

**Wafer Level Mold**

**Back Side MEOL**
SLIM™ Package Assembly Flow

- POP Pillars: 200 µm Pitch or TMV®
- RDL for Memory Interface (if required)
- 30-50 µm bump pitch
- Molded wafer: Thinning as required
- Top of package: RDL if necessary for POP
- Chip Attach & UF
- Wafer Mold
- Carrier Remove & Ball Drop

Interposer with <2 µm L/S BEOL Routing
SLIM™ Test Vehicle – TV1

- Package size: 15 mm x 15 mm
- Top die:
  - Two die, sizes: 5 mm x 10 mm
  - 30 µm pitch minimum
- Flexible TMV® pad pitch
  - 150-400 µm
- Foundry BEOL
  - 2 Cu, 1-Aluminum, 1=RDL backside
- Die information
  - Top die bump count: 4800 (per die)
  - Die to die spacing: 100 µm
- Electrical Characterization
  - Impedance and cross talk

- Package structure

- Status
  - On-going package rel builds
  - One month staggered
    - CLR and BLR
SLIM vs SWIFT Signal Routing Capacity

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SWIFT Platform Technology
Amkor’s Advanced Wafer Fan-Out Platform
SWIFT: Amkor’s Advanced Fan-Out Package

- **SWIFT™**: Silicon Wafer Fan-Out Technology

  - Leveraging existing WLCSP and Assembly infrastructure and materials
SWIFT Value Proposition

- Target Markets
  - Mobile, Networking
  - BB, AP, Logic + Memory, Deconstructed SoC

- Utilizes Existing Bump and Assembly Capability
  - Polymer based
  - Flexible
    - Multi-die and large die capability
    - Large package body capability
  - Advanced die integration
    - Stepper capability down to 2µm line/space
    - Die shift / orthogonal rotation elimination
    - Down to 30µm in-line copper pillar pitch
  - 3D capability
    - Package stack capability using Cu pillars or TMV
Silicon Wafer Integrated Fan-out Technology

- Bottom Multi-layer Formation (Amkor Wafer Level RDL) and Top Ball Drop or Tall Cu Bump
- 200um pitch Vertical Interconnect
- RDL for Memory Interface
- 40um Bump Pitch
- < 0.50mm Total Height
- Carrier Removal
- Top Side Routing or TMV For Memory Interface
- Carrier
- SWIFT
- Carrier Removal
- Wafer Mold
- Chip Attach & UF
SWIFT Key Enabling Process Technologies

- 300mm with mold capability
- Fine L/S RDL ≥ 2um
- Stepper capability
- Multilayer to 3 layers
- Through mold interface (Tall Cu Pillar or TMV)
- > 100um tall CuP bump
- Fine pitch u-bump interconnection
- 40um pitch qualified
- 30um pitch demonstrated
Thank You!
Ron.Huemoeller@amkor.com