Industry Leading High Rate/High Uniformity Blanket Silicon Etch Process for Via Reveal Applications using Rapier XE
## SPTS & Advanced Packaging

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Via Reveal Process Flow

1. **Si wafer**
   - **TSVs**
   - **Glue layer**
   - **Carrier wafer (Si or Glass)**

2. **TSV wafer**
   - **Si is ground short of Cu nodes**

3. **Si etch**
   - **Exposed TSVs with liner oxide intact**
   - **No exposure of Si to Cu in TSVs - Requires oxide selectivity**

4. **Dielectric deposition**

5. **CMP**
   - **Exposed Cu ready for metal re-distribution**
   - **Low temperature Typically <180°C**
SPTS Products for VR Etch

- **DSi**
  - Performance: ≥2.5µm/min, ≤±5%
  - Time: +80%

- **Rapier**
  - Performance: ≥4.5µm/min, ≤±5%
  - Time: +80%

- **Rapier XE**
  - Performance: ≥8.5µm/min, ≤±3.5%
  - Time: +240%

**Highest etch rate**
Best uniformity = Lower CoO + Higher Yield
Rapier XE Module

- ‘Dual Source’ technology
- Recipe driven uniformity tuning
- High & uniform gas dissociation
  - Drives etch rate & uniformity
- ReVia™ *in-situ* end-point detection
  - Down to 0.01% via density
- Wafer edge protection option
  - Protect bond layer & carrier
- Same hardware for TSV etching
  - Interposer, via middle & via last
- Oxide etch capability
  - eg. Spacer etching for via last
<1nm Si Smoothness Post Reveal

- 9µm/min, ±1.8%, 180:1 selectivity

Ra (average) <1nm
Rt (total, peak to valley)<13nm

AFM customer data
ReVia™ End-point Detection

- Built-in compensation for incoming thickness variations
- Copes with low TSV densities
  - <0.011%

Unique & robust end-pointing for any TSV layout or RST variance
End-point Control Saves Money

- **Standard approach**

  Typical flow:
  - 10µm RST
  - 5µm Reveal
  - Total 15µm etch
  - 3µm CVD
  - 4µm CMP

- **Cost Reduced** approach with ReVia™

  Modified flow:
  - 5µm RST
  - 1µm Reveal
  - Total 6µm etch
  - 1.5µm CVD (50%)
  - 1.8µm CMP (45%)

Only available with *in-situ* end-point detection (ReVia™)
Flexibility for 3D-IC Etching

Multiple etches from single hardware set

'Conventional' TSVs

- Interposer TSV
  - 50 x 120 µm <160 nm Sc
- Via Middle TSV
  - 10 x 100 µm <70 nm Sc
  - 5 x 50 µm <6 nm Sc
- Via Last TSV
  - Tapered 100 µm diam No scallops
  - 50 x 100 µm <150 nm Sc
- Via Last TSV Vertical
  - 20 x 100 µm <150 nm Sc

MEMS TSVs (Poly or W fill)

- 8 x 180 µm <200nm Sc
- 4 x 160 µm <50 nm Sc

Via Last ‘Spacer Etch’

- Top
- Mid
- Base
- No oxide

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Summary

- SPTS has highest performance, cost effective, etch solutions for Advanced Packaging
- Rapier XE delivers industry’s highest etch rate & best uniformity
  - \(\geq 8.5\mu\text{m/min}, \leq \pm 3.5\%\) uniformity
  - Lowest CoO, highest yield
- ‘Dual source’ approach allows recipe tuning of uniformity
  - Accounts for incoming residual Si thickness variations
- Smooth Si surfaces are available even at highest rate
  -Ra <1nm
- ReVia™ is the industry’s only end-point detection for VR etching
  - Ensures wafer to wafer repeatability
  - Allows further cost take out due to 1µm tip height capability
  - Capability demonstrated through collaboration with IMEC
- Rapier technology also available for TSV & some oxide etch applications