## Contents

1 Foreword ................................................................................................................................. 2

2 Motivation and Purpose of This Study .................................................................................. 3

3 Introduction to ESD in 3D-IC Packaging .............................................................................. 4
   3.1 Background: ESD Changes .............................................................................................. 4
   3.2 Design and Development of ESD for 2.5D/3D-IC Compared to Single Die Packaging ..... 5
   3.3 Previous Studies – Implementing ESD Protection ......................................................... 5
   3.4 Understanding the Impact of 3D-IC Design on ESD Protection ..................................... 6
   3.5 IC Designers' Requirements and Tolerance for 3D-IC ESD Implementation .................. 6

4 Planning & Analysis ............................................................................................................. 9
   4.1 Wafer / Die Origin Impact on ESD Considerations ......................................................... 9
   4.2 3D Stack Architecture Analysis Tools ............................................................................. 10

5 ESD Threats & Countermeasures .......................................................................................... 15
   5.1 ESD Threats ................................................................................................................... 15
   5.2 Existing Wafer ESD Control methods: .......................................................................... 17
   5.3 Die Stack Assembly & Test .......................................................................................... 18

6 ESD Design Aspects to Consider ....................................................................................... 20
   6.1 Strategy for ESD Design: ............................................................................................... 20
   6.2 Die-to-Die Interface Scenarios ....................................................................................... 21
   6.3 ESD Requirements for Wide I/O .................................................................................. 23
   6.4 TSV I/O Pin Protection ................................................................................................. 23
   6.5 Direct Access Pin Protection ......................................................................................... 24

7 Test Planning: JEDEC documents ....................................................................................... 25
   7.1 Transmission Line Pulsing (TLP) ................................................................................... 25
   7.2 Charge Device Model ..................................................................................................... 25
   7.3 Human Body Model ....................................................................................................... 26

8 Test Impact – Potential ESD Events .................................................................................... 26
   8.1 How to Minimize Potential ESD Events During Assembly ........................................... 26
   8.2 Final Test ........................................................................................................................ 29
   8.3 Qualification ................................................................................................................... 30

9 Failure Analysis ................................................................................................................... 31

10 Case Study from Xilinx ....................................................................................................... 32

11 Summary & Conclusions .................................................................................................... 32

12 Acknowledgements ............................................................................................................ 33

13 Appendix A: Possible Failure Analysis Techniques ........................................................... 34
   13.1 X-ray ............................................................................................................................... 34
   13.2 Scanning acoustic microscopy ...................................................................................... 34
   13.3 IR laser scanning microscopy ....................................................................................... 34
   13.4 Magnetic field imaging ................................................................................................. 35
   13.5 Photon emission microscopy ....................................................................................... 36
   13.6 Lock-in thermography ................................................................................................... 36

References ............................................................................................................................... 37
3D-IC Packaging Electrostatic Discharge (ESD) Guidance

1 Foreword

The Global Semiconductor Alliance (GSA), with approximately 400 corporate members worldwide, fosters a more effective ecosystem through collaboration, integration and innovation. As the voice of the semiconductor industry, GSA provides executive forums worldwide that address global business issues, provide strong networking, and draw industry leaders closer to their OEM, consumer, and government peers. GSA celebrated its twentieth anniversary in 2014.

GSA’s mission is to accelerate the growth of the global semiconductor industry by fostering a more effective ecosystem through collaboration, integration and innovation.

To fulfill this mission, GSA:

1. Addresses the challenges and enable industry-wide solutions within the supply chain, including intellectual property (IP), electronic design automation (EDA)/design, wafer manufacturing, test and packaging.
2. Provides a platform for meaningful global collaboration.
3. Identifies and articulate market opportunities.
4. Encourages and support entrepreneurship.
5. Provides members with comprehensive and unique market intelligence.

Through our Technology Teams, focused on 3D-IC Packaging, Analog / Mixed Signal, Intellectual Property, MEMS, Quality, and Supply Chain, we address critical aspects of semiconductor development and seek solutions to common, precompetitive, problems. We educate the industry and generate impactful deliverables that address difficult aspects of semiconductor development. As such, the membership has a vested interest in understanding and helping resolve issues that impact the global development community. With the advent of movements such as More-than-Moore, Internet of Things (IoT), Trillion Sensors, etc. advanced packaging technologies arise to meet these new opportunities. With opportunities, come challenges; ESD protection during 3D-IC Packaging is one of those challenges.

The ESD Association (ESDA) is a professional voluntary organization dedicated to advancing the theory and practice of electrostatic discharge (ESD) avoidance. The Association has more than 2,000 individual members worldwide. From an initial emphasis on the effects of ESD on electronic components, the Association has broadened its horizons to include areas such as textiles, plastic, web processing, cleanrooms, and graphic arts. To meet the needs of a continually changing environment, the Association is chartered to expand ESD
awareness through standards development, educational programs, local chapters, publications, tutorials, certification, and symposia.

During the 35 years since its inception the ESDA has been promoting many educational opportunities through seminars and tutorials, bringing forward critical ESD issues for the industry through forums and workshops, and facilitating exchange of ESD technical knowledge through the yearly Symposia (EOS/ESD Symposium), Factory Control Symposium, and annual Workshops (the International ESD Workshop). The ESDA has also been funding university research grants to promote constant research opportunities for ESD technology that also add to the collective ESD knowledge. In addition, to look at the critical needs of the industry future, ESDA has established the ESD Technology Roadmap that projects the ESD status into the next decade\(^1\). Finally, the ESDA also has been interacting with the Industry Council on ESD Target Levels; with a mission to establish new and realistic ESD target requirements that allow advanced high speed IC designs and accommodate high performance system designs. These are leading to a paradigm shift in the industry and are expected to have an impact on 3D-IC applications.

## 2 Motivation and Purpose of This Study

For single die packages, electrostatic discharge is well understood, and precautions are taken to minimize the possibility of charge build-up and ESD strikes. In single die designs, I/O (Input-Output) cells contain robust ESD protection circuitry. Additionally, ESD precautions are considered throughout the design, development, fabrication, and assembly/test of devices. As we move toward more dense, vertical packaging, opportunities and challenges exist. Opportunities include smaller footprint, more tightly integrated design, increased performance and decreased power.

Some of these improvements occur through use of less restrictive I/O cell design. In a 3D-IC package, chips are closer together, there are thousands of interconnects, and I/O cell drive strength requirements are significantly reduced. With the majority of interconnects going within the 3D package (die-die), the possibility of an externally triggered ESD event is reduced. Thus, many I/O cells can have significantly reduced ESD protection or perhaps no protection at all.

This new packaging paradigm still requires a thorough understanding of potential ESD events, how to minimize the possibility, and how to react should an event appear to have occurred. This paper will address various stages of the development cycle, for chips designed to be used in a 2.5D/3D package. For each development stage, we discuss challenges and opportunities, potential ESD threats and countermeasures, and compare to individual die development.
3 Introduction to ESD in 3D-IC Packaging

3.1 Background: ESD Changes

The first question to answer: Does 3D-IC integration make ESD a bigger issue than with a single IC design? The answer is multi-faceted, as ESD practices will need to be modified for several reasons: ESD robustness can be stack architecture dependent, and ESD robustness for bare die cannot be guaranteed, as no standards exist for testing. However we can perform full HBM/CDM/TLP (Human Body Model; Charge Device Model; Transmission Line Pulse) testing on a bare die (either by probing on the die or assembling a dedicated test setup). When Thru-Silicon-Via (TSV) are present this becomes extremely challenging and we need to perform micro-probing for on die testing and statistical sampling of which TSV to test. Additional industry experience is required to determine which test should be applied, target levels, etc.

Single die packages have Input/Output (I/O) interfaces that communicate signals to the outside world during functional test and in application usage. The difference for 2.5/3D active dies is that two types of off-chip interfaces exist: External I/O cells that communicate signals to the outside world via interposer, C4 bump, package substrate, or out via package pin; and Die-Die I/O cells, internal to the stack, that communicate between active 2.5/3D die. These die-die I/O cells have no connection to package pins, instead driving signals via micro-bumps, interposer, and 3D traces.

Both types of I/O must be protected against electrostatic discharge that can permanently damage an active die and, in this case, render the 3D stack inoperable. External 2.5/3D I/O have ESD design that is similar to that of monolithic die with enhanced CDM protection features to address the larger CDM peak current of 2.5/3D packages. Die-die 2.5/3D I/O may have significantly leaner ESD protection with much smaller footprint.

The criteria for ESD design is to protect against possible ESD exposure during assembly of various die into a 2.5D or 3D package. ESDA standard S20.20 regulates 2.5/3D assembly lines with regard to the ESD environment. This allows designing die-die I/O to meet only 100V HBM while external I/O may often be qualified to meet 200V CDM and 1000V HBM.

One proposal is to reduce ESD burden for each die for those I/O that connect through TSV and to the package ball, because each die will share ESD protection capability. This paper recommends a reduced (compared to current stand-alone die package) ESD protection specification for dies in a 3D-IC package. This helps minimize ESD over-design in an attempt to be qualified identically to single die ESD specifications. This should be beneficial throughout development, creating smaller/cheaper die, while providing the ability to achieve higher performance with lower IO drive strength.

Developing a 3D-IC ESD standard would be beneficial to both vendor and final product owners as:
The vendor can save die area, while not customizing die individually for each customer’s ESD requirements, and
Final 3D-IC product owners can source from multiple vendors, with consistent ESD performance

3.2 Design and Development of ESD for 2.5D/3D-IC Compared to Single Die Packaging

ESD design strategies for standard IC are well understood. The ESD design rules, together with the corresponding I/O ESD library are typically available in a Process Design Kit (PDK). EDA tools are available to assist in the design of full chip ESD protection strategy and ESD test standards exist.

For 2.5D solutions, the ESD design strategy is less clearly defined. In general, the same ESD design rules as for standard IC apply; however, one could lower the ESD specifications for internal, die-die I/O. Lowering the ESD specification will result in a smaller ESD area requirement. Testing a die which ends up in a 2.5D interposer package is not clearly defined. As described later in this paper, wiring out each I/O (both die-die and external) on a test board and performing regular ESD testing is a possible solution.

For a full 3D design, e.g. Memory on Logic or Wide Memory I/O test cases, providing complete ESD protection on each of TSV (4096 for wide memory I/O) would result in a very large ESD area penalty (ESD devices and ESD routing), even with the lowered ESD I/O spec from 2.5D. An option could be to assemble the stack in a well-controlled environment and rely on the intrinsic ESD robustness of the TSV driver circuit to carry / dissipate ESD current. A good power delivery network must be designed so that it can be optimized for ESD.

3.3 Previous Studies – Implementing ESD Protection

At the EOSESD 2012 symposium, IMEC studied the use of ESD protection devices placed inside the Keep-Out Zone (KOZ) of Through Silicon Via (TSV) in 3D Stacked Integrated Circuits. In this work, potential ESD threats from specific 3D-IC processes, such as wafer thinning and bonding were discussed. Secondly, a design concept of utilizing the KOZ of TSV for ESD protection devices was proposed. Through several different configurations, “IN” or “OUT” of KOZ with different numbers of TSV, the measured results show that ESD protection devices can be safely implemented inside the KOZ. Another ESD protection strategy, safe ESD paths, was proposed for preventing CDM (or CDM-like) ESD events in 3D-IC applications.
3.4 Understanding the Impact of 3D-IC Design on ESD Protection

Die designed specifically for 3D-IC stacking will have two types of I/O and therefore two ESD protection schemes:

1. Full ESD protection for external I/O (designed to connect outside 3D package)
2. Limited ESD protection for internal, die-die, I/O (designed to connect within the 3D package)

Die-die I/O cells will have decreased drive strength requirements, due to shorter distances between closely stacked die. Therefore, these die can potentially support:

- Faster clock capability
- Smaller die size due to reduced I/O ring size
- Larger number of interconnects, leading to higher performance
- Lower power dissipation and therefore less thermal extraction requirements

3.5 IC Designers' Requirements and Tolerance for 3D-IC ESD Implementation

Fundamentally, there are two types of 3D-IC ESD exposure to be considered. One is illustrated in Figure 1 which shows a diagram representing a finished package test in a CDM tester such as Thermo’s Orion 2. Two die, A and B, are shown side by side in a package with each die having a certain capacitance to the tester’s field plate. An interposer could be present but is not shown. Also shown is a die to die ground package trace connection which has some amount of inductance and resistance. Both die are charged to some voltage relative to the field plate. In this example the Vdd node of Die B is struck by the CDM probe which connects Vdd to the CDM tester’s ground through an impedance, Zcdm. The main current discharge flows from Vdd through the BigFET or RC clamp and discharges the assumed negative charge on Die B’s capacitance, CcdmB. Current also flows through the ground interconnecting trace to Die A’s capacitance, CcdmA and discharges it as well.
A potential secondary discharge path for the charge on die A is through the gate oxide of the receiver inverter in Die B, through the signal trace from die A to die B, through the driver PFET’s drain-body diode of Die A, and through power bus BigFETs and capacitance to the ground of Die A. In this scenario the gate oxide of the PFET can be ruptured since the oxide is weakly conductive before failure. The voltage drop between the two die is dependent on the current magnitude and slew rate of the cross Vss trace which generates a voltage drop of IR+Ldi/dt. If this voltage drop in conjunction with voltage drops of the internal bus resistances and Die B’s BigFET is large enough then the receiver’s PFET gate will rupture. Compounding the threat is the fact that designers like to use low voltage core transistors for chip to chip signaling to increase speed and reduce power. Core transistors in advanced technologies have gate dielectrics that can rupture with only a few volts in the CDM event time.

To allow for a larger voltage difference between the two die during an ESD event, a chip to chip ESD attenuator is used consisting of a resistor and two diodes placed on the input as shown in Figure 2. The circuit is commonly referred to as a secondary clamp and is used for cross domain signaling within a single chip as well. In this scheme the series resistor can be used to absorb the voltage drop between the two die. The RC product of the resistor and the capacitance of the receive input and diodes can be as small as 10pS thereby keeping the delay small. A more compete treatise on this subject can be found in^5.
Figure 2: Same package as shown in Figure 1 but with a secondary or attenuator clamp inserted in front of the receiver

The second case of ESD exposure does not involve a standardized qualification test but is encountered in assembly. As a die is brought into contact with a package substrate or another die there can be a potential difference between the die and the attachment target. This ESD stress will be smaller than that associated with the standardized qualification package test but can still cause damage to unprotected bumps given the sensitivity of advanced processes.

Figure 3 shows an example of two die that are placed on an interposer as before. The first die placement, die B, should have no problem since the signal traces connecting to the signal bump have very little capacitance and, therefore, little current will flow through the signal bump as attachment is made assuming that Die B and the interposer are at different potentials. However, when die A is placed its first bump to touch the interposer trace could be a signal trace connected to die B which can be connected to the interposer ground. Thus, there can be a significant amount of capacitance between Die A and Die B and the interposer. If the signals use core transistors for driving and receiving and are in an advanced technology the maximum voltage tolerance between die can be as little as 3V. If the voltage difference is 10 to 15V the secondary clamp can keep the receiver safe by attenuating the voltage and slowly equalizing the potential on Die B to that of Die A. However, if the voltage is large, say 50V, then a primary clamp has to be added, such as diodes Dpp and Dpn. Depending on the voltage difference, primary diodes can add a lot more capacitance than just secondary diodes. Thus, the data rate between die depends in
part on low potential differences during die assembly. It is essential that die assembly equipment specifies the potential difference and even discharge waveforms for design.

![Diagram showing die A and die B with CcdmA and CcdmB capacitances and voltage differences V1 and V2.]

**Figure 3:** Same package as shown in Figure 1 but with both primary and secondary clamps. The switch represents a signal trace coming into contact with a chip bump.

In conclusion, the die interface involved with 2.5/3D packages can be readily designed for the CDM qualification test using existing methods. However, die assembly ESD is presently not specified and can’t be designed with any precision. Design overkill is not recommended as an option, as the data rate performance will be seriously impacted.

## 4 Planning & Analysis

### 4.1 Wafer / Die Origin Impact on ESD Considerations

One concern with 3D-IC packaging is integrating die or wafers from different sources. While the memory stack may come as a certified unit, mixed signal dies, sensors, logic dies, wafers, etc., will likely come from multiple sources. Thus the system architect / package integrator may not have access to chip design criteria. Wafer level testing capability needs to be enhanced to ensure Known Good Die (KGD) or Probably Good Die are delivered to the 3D stack integrator. There is limited commercial wafer level testing for HBM; test methodologies need to be developed for common use. Wafer level CDM testing of individual die is not possible; therefore, there is no equipment for this type of testing.
Potential ESD build-up events to be considered include: Wafer Backside Thinning, Wafer Wet Grind or Dry Polish. Dies intended for 3D-IC packaging will undergo wafer thinning to expose TSV, complicating wafer handling requirements. Knowledge of techniques is required for Wet Grind, where the liquid can lead to charge build-up, and Dry Polish which is susceptible to charge build-up.

These issues require careful analysis and planning by the system architect (this term is used generically to mean the organization that ships the 3D-IC product to the customer and likely has failed parts return and Failure Analysis responsibility). Depending on the business model, these activities may occur at the wafer fab, at an intermediate vendor, at the assembly and test facility, or at a system aggregator/integrator.

### 4.2 3D Stack Architecture Analysis Tools

The demands of scaling form factors, performance targets, and cost constraints are increasing the need for three-dimensional integrated circuit (3D-IC) stacked-die designs. However, chip designs using TSV in 3D-IC or silicon interposer-based technology, as shown in Figure 4, require advanced modeling, simulation, verification, and debug capabilities in order to meet the demands of low-power mobile, high-performance computing, consumer, or automotive electronics markets. There are challenges in meeting these demands including verification of the integrity of power, signal and reliability. In particular, this paper focuses on ESD integrity aspects of 3D-IC design.
The ESD integrity check for a 3D-IC shares the same HBM/CDM test requirements of a single die/package plus IEC61000-4-2 system-level test including the single die/package. However, the passing voltage level for HBM/CDM and system-level test for different application segments are still under committee review. Illustrated in Figure 5 are the industry common HBM/CDM requirements for an SoC.

### New Recommended HBM Classification Based on Factory ESD Control

<table>
<thead>
<tr>
<th>HBM Level of IC</th>
<th>Impact on Manufacturing Environment</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 KV</td>
<td><strong>Basic ESD Control</strong> methods allow safe manufacturing with proven margin</td>
</tr>
<tr>
<td>1 kV</td>
<td><strong>Basic ESD Control</strong> methods allow safe manufacturing with proven margin</td>
</tr>
<tr>
<td>500 V</td>
<td><strong>Basic ESD Control</strong> methods are required</td>
</tr>
<tr>
<td>100 V to &lt;500 V</td>
<td><strong>Basic ESD Control</strong> methods are required</td>
</tr>
</tbody>
</table>

**Basic Programs:** Include wrist straps, grounded work surfaces, and safe packaging materials – and are safe with proven margin to 500V.

**Detailed Programs:** JESD625B has a scope of 200V, but does not have a footwear-flooring system test for personnel grounding.

- Processes compliant to ANSI/ESD S20.20 or IEC-61340-5-1 allow handling and manufacturing of ICs even as low as 100V HBM.

⇒ Published as JEP155
Figure 5: Typical HBM/CDM Requirements for an SoC (may be different for a 3D-IC; under committee review)

A typical phase-by-phase ESD integrity check flow for SoC or 3D-IC development is illustrated in Figure 6. While the HBM test results on an interposer-based 3D-IC will be comparable to that of a single die/package test due to the common TSV path, the CDM test results will often be worse due to the larger size of the 3D-IC package and conductive paths between multiple die.

<table>
<thead>
<tr>
<th>CDM classification level (tested acc. to JEDEC)</th>
<th>ESD control requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CDM} \geq 250V$</td>
<td>• Basic ESD control methods with grounding of metallic machine parts and control of insulators</td>
</tr>
</tbody>
</table>
| $125V \leq V_{CDM} < 250V$                       | • Basic ESD control methods with grounding of metallic machine parts and control of insulators +
  • Process specific measures to reduce the charging of the device OR to avoid a hard discharge (high resistive material in contact with the device leads). |
| $V_{CDM} < 125V$                                | • Basic ESD control methods with grounding of metallic machine parts and control of insulators +
  • Process specific measures to reduce the charging of the device AND to avoid a hard discharge (high resistive material in contact with the device leads) +
  • Charging/discharging measurements at each process step. |

Published as JEP157
Figure 6: Simple ESD Verification Flow Mapped to Sample IC Design Flow and Referenced to Rules as illustrated in ESD-TR18.0-01-14 From ESDA

Compared to a single die/package IC, HBM for a vertically stacked 3D-IC, as shown in Figure 7, will in general be better as the TSV will slow the discharge rate.

Figure 7: Detailed View of a Vertically Stacked 3D-IC

The circuit shown in Figure 8 is an exception to this rule. In contrast, the CDM for a vertically stacked 3D-IC could be worse with the additional charges from the top die(s).
Figure 8: Top Die power clamp is turned on before Bottom Die power clamp turns on, for the condition of $V_{t1} > V_{clamp} + I_{hbm} \times R_{hbm\_path}$. This will result in higher accumulated voltage for the nodes on the discharge path.

The requirements for EDA tools for 3D-IC ESD integrity check are similar to the ESD check on a single die/package design. The package pins of a 3D-IC will go through the same ESD stress test specification for either HBM or CDM. The verification of appropriate ESD protection structures from a topological (schematic-level) perspective, while ensuring that ESD structures are not missing or inappropriately sized still needs to be done. Automation of these tasks will enable consistent and repeatable results. The differences lie in the need to handle all dies, and packages in a 3D-IC together, for topological (schematic-level) checks and Resistance and Current Density check as per JEDEC specifications, as shown in Figure 9.

Figure 9: Typical Resistance, Current Density, and Voltage Check in Static ESD Integrity Analysis

Static or dynamic ESD checks may be needed for a 3D-IC, depending on the manufacturing and assembly of the die stack. An increased number of dies may contribute
to a single CDM event. Such an event could cause CDM issues not detectable by Resistance/Current Density (R/CD) checks in vertically stacked dies in isolation.

However, since the individual die of a 3D-IC design may come from multiple vendors, incomplete data for a 3D-IC is common and hence a problem from an ESD integrity checking point of view. Data sharing through models may become necessary to perform comprehensive ESD analyses of these stacked die systems\(^\text{13}\). These die or package/PCB models should be a compact and accurate representation of dies/package/PCB. Alternatives would require the independent verification of each standalone die, while providing special handling of interface layers and circuit structures that traversed multiple die\(^\text{14}\) to compensate for elements that couple across dies in a modified 2D verification methodology. Such an alternative may create systems that offer greater scalability for verification, but require greater care for boundary conditions. See Figure 10.

![Figure 10: Modified 2D Verification; Multiple Stacked Dies](image)

An example of a die or package/PCB model would be an ESD die compact model containing a passive component, a current signature that describes the port current of a chip for a specific scenario, and ESD diodes/clamps in an I-V Piecewise Linear model as demonstrated in\(^\text{16}\). This die model can be used together with other die in a 3D-IC along with a passive package model for R/CD check. This is particularly true for 3D-IC designs to facilitate a methodology flow, providing a verification platform for stacked-die designs that will meet the requirements for ESD integrity check.

## 5 ESD Threats & Countermeasures

### 5.1 ESD Threats

Charge build-up can accumulate at several points throughout wafer fabrication and transport, or assembly and test. The table below lists several areas where charge (C) build-up can occur. This is followed by a table showing potential for an ESD event strike (S).
<table>
<thead>
<tr>
<th>Threats</th>
<th>Charge</th>
<th>Precaution / Countermeasures</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD buildup due to wafer thinning</td>
<td>C</td>
<td>Ionization before bonding to substrate</td>
</tr>
<tr>
<td>Static Charge is stored on unshielded conducting surfaces</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>TSV Reveal</td>
<td>C</td>
<td>Implement S20.20 safeguards</td>
</tr>
<tr>
<td>Wet Grinding</td>
<td>C</td>
<td>Less susceptible to charge buildup</td>
</tr>
<tr>
<td>Dry Polish</td>
<td>C</td>
<td>More susceptible to charge accumulation</td>
</tr>
<tr>
<td>Charge stored on</td>
<td>C</td>
<td>Discharge current may not be confined to a single die</td>
</tr>
<tr>
<td>• Metal parts of package</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Interposer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Die closest to field charge plate (often, the top die in the stack)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>If charge accumulates, then an ESD Event (Strike – S) is possible, as noted at various steps below</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die-Die Bonding</td>
<td>S</td>
<td>Place small ESD clamps at receiver inputs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Provide a common ground plane</td>
</tr>
<tr>
<td>Package-Package Stacking</td>
<td>S</td>
<td></td>
</tr>
<tr>
<td>First TSV Contact (Figure 9)</td>
<td>S</td>
<td>Ground corners, edges, center TSV</td>
</tr>
<tr>
<td>Some ESD events would require charge transfer from VSS and VDD nets on the top die to the VSS net on the die that connects to the external pins</td>
<td>S</td>
<td></td>
</tr>
<tr>
<td>Die-die I/O are subject to overvoltage stress</td>
<td>S</td>
<td></td>
</tr>
<tr>
<td>Magnitude of voltage stress is affected by</td>
<td>S</td>
<td>Proper Power Distribution Network Design</td>
</tr>
<tr>
<td>• Rail clamp design and placement on the dies</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Single vs. multiple power domains</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Power distribution network (esp. ground net)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Five. Two Existing Wafer ESD Control methods:

To date there are very few controls methods that are used in wafer fabs. The controls that are in place are typically used for contamination control due to electrostatic attraction.

The majority of the industry does not consider a wafer to be an ESD sensitive device until there are exposed connections. In order for devices to become sensitive to ESD events two things must occur. First there must be a difference in voltage between two objects; second, the two objects must come into contact through a conductive connection. In the case of wafers, there are no exposed connections until the very end of the line and therefore they are not sensitive until then.

With 3D this changes somewhat. The connections or TSV must be exposed much earlier in the process. This process typically has a wafer mounted to a substrate and then thinned or ground to expose the TSV. Two devices are then joined making contact. This is the step in the process where it is essential to keep the two devices as close in voltage as possible.

Once the connections or TSV are exposed, the risk for a dangerous discharge is much higher. Although the risk for an operator to touch these connections is pretty low, ESD controls as described in ANSI/ESD S20.20 and IEC 61340-5-1 standards should be followed. The premise of both of these standards is to control charges on conductors (and people), develop a plan for insulators, and use protective packaging for transit and storage. Furthermore the respective risk of every single process should be analyzed as described in chapter 8.1.

Consideration of the process before the TSV are exposed is unique to 3D-IC. As the typical process bonds the wafer to a substrate, such as glass, before the wafer is thinned, that process must be addressed. In this process one must assure that the wafer and the substrate that the wafer is being bonded to are at very low potential before the bond
process. This can be accomplished by using ionization before the wafer and substrate enter the bonding tool.

The consideration here is that, if the substrate becomes charged, then after the bond process, the substrate will become inductively charged and remain charged until the TSV is exposed. Then any contact with a conductive object or the device it will be bonded to will cause a discharge. Once the substrate is bonded to the wafer, the bonded wafer will not be able to be discharged by ionization. The same consideration must be given when the device is separated from the substrate.

5.3 Die Stack Assembly & Test

The information in this section can be applied to die stacking using intimate bonding, copper pillar, or any form of solder bumping or micro-bumping technology. Further, this discussion is not limited to 3D assemblies, but can be applied to 2.5D die to wafer or die to substrate assemblies as well.

There are two different basic standards that apply to die stacking. In the first case, dies are foundry assembled and, like wafers, are assumed not to be exposed to ESD events during assembly. As long as the final assembly has no exposed I/O that are not fully ESD protected, one should refer to and apply the wafer level standards as specified in section 5.2.

In the second case, dies are assembled and tested in a non-foundry environment. The dies in this case must have adequate ESD structures that prevent die damage during machine assembly, but care must be taken to minimize the environmental hazards. The construction of die test, handling, and attach machinery should make all reasonable attempts to reduce discharge event issues by ensuring that machinery, robotics, probe cards, assembly handing trays, and any other related equipment are at the same potential and, when possible, have minimal both DC and AC electrical impedance between them. In no case should there be electrical isolation. The AC impedance frequency that is most relevant for the prevention of damage is that of the machinery’s AC power source, such as 50 or 60 hertz. The recommend impedance is less than 1000 ohms.

An adequate ESD discharge connection can be accomplished by presenting conductive backside die surfaces. Best practices would provide for such die connection but manufacturing and design limitations may prevent this. In some cases the die itself may not have a low impedance path from the handling equipment to its own internal ground plane. In these cases, the target assembly should be connected to the common handling ground with an impedance of between 100 and 5000 ohms. The impedance will act to minimize any peak device currents.
5.3.1 Relevant classes of ESD protection both assembly and test processes

5.3.1.1 Minimum protection case

At a minimum, all I/O on the die must have secondary diode protection. The ESD discharge protection level of an antenna diode structure is typically no more than 2mA. If this is the only ESD structure present for the least protected input, the die must be handled either in accordance with the above wafer handling requirements or else by its backside with the backside conductively attached to the device ground plane.

5.3.1.2 Nominal ESD protection case

In a nominal case, the device will have minimal standard ESD protection on each I/O as well as adequate power rail clamps. The ESD structures should be capable of handling a discharge current of 100mA.

The following reference information is provided for guidance and may not reflect the specifics of any particular semiconductor process. The designer must conform to the specifics of their device process.

The minimum diode structures for such a discharge require a nominal 10um of diode periphery with adequate contacts and metal interconnect to prevent the maximum voltage at the pad from exceeding the gate oxide failure voltage level. Calculations for the interconnect must account for the voltage drop across the interconnect resistance for the entire relevant discharge path as well as the voltage drop of the diode structure or whatever other voltage clamping structure is employed. For purposes of ESD discharge, 10x nominal current handling is typical.

5.3.1.3 Best ESD protection case

If the device I/O and power rail clamping structures are all designed for typical packaged die applications, where these interfaces are subsequently connected to a circuit card or equivalent, then normal die packaging and assembly standards can be applied.

5.3.2 Multiple die stacking

When multiple dies (>2) are stacked, the dies should share a single common ground plane structure. In some cases this is not desirable, as noise isolation is required. In these cases, the isolated planes should have crisscrossing voltage clamps between the isolated rails. The clamps need to be present in every die that has relevant rail connections other than metal-only-connected passthroughs with antenna diodes. It is best practice that each die in the stack have rail clamps for all rails, but all rail clamps should be present in at least the first (base) die handled in the assembly.

There may be internal, substrate-specific signals that penetrate intermediate layers before reaching a true ESD terminating structure. In best practice, ESD structures are always on the first substrate that has physical connections to the outside world. When the terminating ESD structure is not on the first substrate, one may wish to minimize the loading and still
protect intermediate structures such as TSV. To do this, the intermediate non-ESD protected wiring structures should use a resistive (>1000 ohm) antenna diode structure to prevent damage during processing and assembly while not failing during an actual ESD event on the final assembly. A stacked antenna diode might be an adequate alternative.

5.3.3 Multiple substrate connections to an external signal

When multiple substrates are connected to an external signal, best practice is to protect each I/O with a complete ESD structure. This may present an unacceptable load or other undesirable circuit restrictions. If the external signal-related I/O connections share a power rail such as ground, the ESD structure should be placed on the most susceptible I/O interface, normally the thinnest gate oxide layer. If the I/O interfaces do not share a related power rail, the rails must be crisscross clamped and the effect of the clamps on the apparent worst case ESD voltage must be taken into account on each I/O. If crisscross clamping is not acceptable, there is little choice but to protect each I/O as if it were there only structure present on the node that would mitigate the ESD event.

6 ESD Design Aspects to Consider

6.1 Strategy for ESD Design:

In designing for the 3D-IC environment, one must consider many things that a planar chip designer would not encounter. Will the chip have I/O that go external to the stack, I/O that only go die-die, or a mix? How does this impact the I/O ring and die size? Is die size driven by a need to match specifications set by the package integrator? I/O drive currents are potentially reduced, due to shorter drive distance, but stack CDM current may be larger due to increased 3D-stack circuitry and a larger number of interconnects.

A system level approach, similar to that required in designing an SoC, will be required for Power Domain Crossings chip to chip.

FMEA (Failure Mode and Effects Analysis) must now consider additional attributes, such as die stacking order, the possibility of no die level ESD testing, when and where testing will occur in the assembly flow, and how failure returns will handled.

Coordinating ESD design amongst all parties may be required, similar to system level design for Charged Board Model

1. Cross-Chip Interconnect is more like cross-domain signaling for package level exposure but is more like external ESD exposure for die assembly
2. Full up external ESD protection is most likely not necessary

EDA tools must perform component-level, not just die-level, ESD analysis. New EDA tools are needed for analysis and design optimization.

- Analysis should focus on Power Distribution Network (PDN), pad cells, and die-die I/O
It is very important to consider power / performance / ESD reliability trade-offs

- ESD loading will compromise performance (or require more power) for some (not all!) channels
- Need to understand where protection is needed and how much

Quickest, safest approach:

- Design PDN to be the primary discharge path
  - Keep ESD currents away from die-die I/O
- Place small ESD clamps at receiver inputs
  - This is a proven approach for stacked-die Silicon-in-Package

Or, perform CDM analysis for every pin, zap to check if node voltages at any die-die I/O exceed safe limits

- Use ESD clamps where hazards are identified, or redesign the PDN to reduce voltage drops
- Proven tools for 3D-IC stack ESD analysis do not currently exist

Optimize 3D-IC ESD protection network

- Ensure that the rail clamps on the various die trigger at the same time
  - Share the stress current between the die
  - Resulting ESD robustness expected to be very high
- Or, ensure that PDN design provides sufficient full-system voltage clamping without rail clamp instantiation on dies 2 – N.

Figure 12: The Key to robust CDM design will lie in a correct ESD architecture for all power/ground domains of the 3D stack as a whole.

6.2 Die-to-Die Interface Scenarios

Possible Development Flow Scenarios (Note: There are myriad variations, only a few are given):

- All dies designed by same company, fabricated at single foundry, assembly under foundry control
- Same as A, but foundry outsources Assembly and Test
Die designed by multiple companies, same foundry, same process. Foundry responsible for final product.

Same as C, except foundry outsources Assembly & Test. Coownership of final product.

Multiple design houses, multiple foundries, multiple process, OSAT responsible for A/T and final product.

Same as E, except third party (system integrator, etc.) coordinates entire flow and is responsible for final product.

Each of the scenarios will have different potential charge build-up possibilities and ESD strike opportunities. The party responsible for the final product, and therefore customer and Failure Analysis liability, will have to determine the most viable development flow.

**2.5D / 3D TSV Assembly Flow**

Figure 14: Sample Assembly Flows

Courtesy of Amkor Technology
6.3 ESD Requirements for Wide I/O

At EOS/ESD Symposia 2014, a 3D TSV stacked demonstrator IC for memory applications with a Wide I/O data bus was evaluated under ESD stress. CDM testing was used to test the robustness of the 3D system against ESD stress during the die-stacking process.

It was shown that the junctions in the mini-I/O transceivers sufficiently protected the chips throughout the 3D chip stacking process, proven by the fact that the wide I/O demonstrator properly functions and operates at the specified performance. The CDM stress test outlined in the aforementioned paper was carried out in a post-processing stage. The device exhibits error-free operation for the very high CDM stress conditions of 1.6 kV which corresponds to a peak current of 20 amps, indicating high reliability in a real environment.

The ESD protection methodology used relies on standard protection of I/O cells on each die in the stack (as provided in the PDK of the technology used), and on a good VDD VSS connection between the stacked die using sufficient TSV. The individual Wide I/O TSV (4,096 count) have no dedicated ESD protection design, other than the inherent drain junctions in the drivers, which could conduct ESD current. A very high CDM protection level was obtained and is ensuring sufficient CDM ESD robustness for both the die-stack assembly and the later handling of the IC.

6.4 TSV I/O Pin Protection

As documented in previous sections, ESD protection strategy involves consideration of many factors. The main issue always is the unknown I/O design and any existing ESD protection on the other interfacing die. Here, the example of an SoC stacked with a memory die is presented to illustrate the perspectives. As long as it is known that the TSV pillar can handle the ESD target current level, the ESD design should safely focus on the main die independent of the knowledge of the other die(s). Therefore the design should meet full ESD protection for all TSV nets that touch package balls.

In the case of die-die I/O, whether through TSV or directly connected, there is no connection to an outside package ball and full ESD protection is not needed. However, for CDM reliability during die stack assembly, some sort of protection is recommended\(^\text{19}\). The small diodes at the interface (shown in Figure 15) can serve this purpose but the question remains how small should they be in order to provide minimum loading capacitance (typically <100fF) and allow desired speed performance. Depending on speed requirements that restrict this design, CDM currents can be obtained that translate to 100V or better CDM level. This in turn is determined by the hybrid package capacitance.

As the TSV pillar pitch decreases with new process nodes it may become more difficult to implement the dual diode approach in the TSV array as shown in Figure 15. The main difficulty encountered is that the TSV array cannot block routing metal used for the logic cores so the design team must ensure that ESD paths have sufficient metal. Using a
"failsafe" (no diode to VDD) ESD structure on the internal TSV nets may make the TSV cell less congested by removing the connection from ESD diode to supply. For example, it could be a small 3-diode string from I/O to VSS.

Figure 15: TSV I/O Protection Method. A small pair of diodes can serve as useful CDM protection during die stack assembly.

6.5 Direct Access Pin Protection

In the case of Direct Access (DA) I/O pins, full ESD protection should be implemented. This would serve as the main protection during package handling and testing could be directly done on the top die package pins. A typical implementation is shown in figure 16.

Figure 16: Direct Access Pin Protection Method. A full sized ESD clamp can be implemented.

There is one caveat in the Direct Access pin design case. It is not known exactly what is on the other side, whether the implemented ESD clamp can be compatible with the interface I/O devices, and also the degree of interaction if there is an ESD protection on the I/O. Since all of this could be a large potential unknown, a simple ESD clamp such as a forward mode 3-Diode string from DA to VSS, along with a negative substrate diode, could resolve the minimum ESD protection requirement. If the interface I/O has a diode to its VDD along with a VDD to VSS clamp then sufficient protection can be obtained. On the other hand, if the I/O has a snapback protection device its trigger will depend on the voltage buildup from the 3 diodes initially turning on. In the worst case if there is no protection on the interface I/O the buffer devices are still protected by the 3 diode string. With this approach at least 1kV HBM and about 200V CDM protection can be achieved for the DA pins.
In this regard the Direct Access (DA) pins are involved in testing the top die directly.

7 Test Planning: JEDEC documents

7.1 Transmission Line Pulsing (TLP)

Transmission Line Pulsing (TLP) is an established characterization method to extract the high current behavior of ESD protection elements as well as on-chip interfaces. The test is performed by forcing a trapezoidal current pulse waveform into one pin of the device under test (DUT), while the complementary pin of the DUT is connected to ground. The voltage response is detected. A typical set-up consists of a 50 Ohm transmission line for the injection of the pulse. Either the complete voltage waveform or the plateau level of current and voltage waveforms are monitored. A leakage measurement after each pulse allows one to determine the destruction level, if the leakage current has significantly increased. Typical pulse duration is 100 ns. Pulse rise time between 100ps and 10ns can be used.

Often the device investigation is complemented by a so-called very fast TLP (vfTLP) with pulse length of 1 to 5 ns. Significantly high current levels can be injected under vfTLP conditions; this allows investigation of failure mechanisms of dielectric breakdown on the IC.

7.2 Charge Device Model

Charged Device Model (CDM) testing is a standard qualification test method for packaged ICs. The test methodology is described by the joint JEDEC/ANSI/ ESDA CDM standard JS-002-2014. For today’s manufacturing and handling environment CDM is the most relevant stress test method. The stress test is a discharge of a charged package through a single pin. The stress parameter which leads to the on-chip failure is the peak current. The peak current depends on the package used\(^2\). As the component is qualified in terms of CDM voltage, which is an equivalent voltage level of a CDM simulator, a silicon die will perform in different packages differently. Typical CDM qualification target levels for package pins are 250V, which amounts to 1A to 6A of peak current.

7.2.1 Relevance for 3D ICs

The discharge of a charged die through one exposed pin is relevant in 3D manufacturing. This discharge scenario is tested at IC level by CDM testing, where the actual stress level largely depends on the package size. On die level, the test for fast discharge through one pin has to be revisited. A correlation between robustness of a die in a 3D manufacturing environment and the CDM robustness when it is packaged cannot be drawn. As discussed above the relevant physical parameter is the discharge peak current. No standard test method for die testing has been implemented yet, but characterization test methods on wafer level are in use based on the concept of TLP, which allow the extraction of a critical

7.3 Human Body Model

Human Body Model (HBM) test is the most common standard qualification method to evaluate ESD robustness of ICs as described in the JEDEC/ANSI/ESDA standard JS-001-2012. A typical qualification level is 1kV, which leads to a discharge current of 0.7A through the stressed pin, while a group of pins is connected to ground. Due to the longer duration of the pulse of > 100ns the typical failure mechanism is thermal destruction. In many instances the failure signature can reproduced by 100ns TLP stress testing.

7.3.1 Relevance for 3D ICs

Thermal fails due to pin to pin discharge through a die as probed by HBM model is a questionable discharge scenario for 3D-IC stacking in general. There is hardly any handling step for bumped I/O which can lead to such a discharge. However, wire-bonded 3D-IC stack might experience this. ESD control measures according to S20.20 allow safe handling of parts with a 100V HBM withstand level. This is considered to be fully sufficient for die-to-die handling, if qualification for a HBM level is required at all.

8 Test Impact – Potential ESD Events

8.1 How to Minimize Potential ESD Events During Assembly

Die level or incremental die stack testing should be done with the care required by the ESD structures present at that assembly level. If internal nodes are present that are only protected with antenna diodes, the die or partial 2.5/3D assembly should treat all inputs as highly ESD sensitive and the most stringent ESD controlled environmental practices should be observed. But what are the right ESD control measures? It is definitely a good idea to ground an operator, although they will never be able to touch a sensitive structure on the die/wafer. The simple reason is to avoid that an ungrounded operator is introducing any charge to wafers or wafer carriers that could be a problem in one of the automated process steps.

The greatest risk is that a die/wafer becomes charged and discharges into the other die/wafer while stacked. An often used practice is not to care for the charging but to avoid a hard discharge by using a dissipative substance for the material that comes into contact with potentially charged devices. This would limit the discharge to an non-critical value. This is not possible where we have die to die contact. Therefore, charging of the device has to be avoided or at least reduced to an non-critical value. There are several ways to reduce potential charging:
• **Ground the object under consideration:** e.g., if the top die is placed onto the bottom wafer using a placement tool with a suction cup, the suction cup should be made of dissipative material and grounded whenever possible. This would drain off the charge in a controlled way and avoid a potential difference to the bottom wafer. Of course the bottom wafer also has to be uncharged.

• **Use ionization to reduce charging:** if the top die and/or the bottom wafer cannot be grounded, it is common practice to use ionization to neutralize charge on the charged object. It has to be considered that neutralization needs time and that the ions need be able to reach the charged object.

• **Change the process to avoid or reduce charge generation:** sometimes neither grounding nor ionization can be used; in this case a change of the process has to be considered, e.g. by reducing the speed of separation or intimacy of the contact.

Which technique above is to be used to reduce this CDM-like risk can only be decided after analyzing the respective process steps.

### 8.1.1 Basic idea of CDM protection

Basically there are several ways to analyze CDM-like risk. Some approaches are already published to give the end-user a guideline in analyzing the CDM-like risk or the process capability of the respective production line. The US ESD Association is also preparing a Technical Report for publication in the near future.
The basic idea of these approaches is shown in figure 17.

![CDM risk analysis flow](image)

**Figure 17: CDM risk analysis flow**

The respective measurements will then answer three main questions:

1. What is the process capable of protecting in relation to CDM?
   a. Note: Even if the values for CDM robustness determined during device level testing are not directly comparable, we know by experience that we normally have no automated handling problem in a controlled line when the measured charging values do not exceed the CDM robustness values.

2. Where are the ESD problem areas in the process, and what risk do they pose to CDM sensitive structures?

3. How effective can any changes to the process be for controlling CDM risks of sensitive items?

### 8.1.2 Process related risk analysis

While doing the investigation of device charging, it also has to be taken into account whether or not these charging values are dangerous for the object; i.e., it has to be analyzed whether the charged object “sees” a contact to ground (or another conductive object on a different potential), which is introducing a dangerous hard discharge (CDM like event) to the charged object. If that’s not the case, the charging will normally not cause any damage to the object (electrostatic problems like attraction of particles by charged objects will not be discussed here).
This results in an analysis of every single process step by asking the following questions:

- Is there charging of the object being manufactured?
- Is there a chance for a hard discharge in this or the next process step?

If there is no charging, there is no possibility for a hard discharge. If there is no hard discharge, there is normally no possibility of CDM-like damage. More details are described in\textsuperscript{21}.

8.1.3 Process Capability & Transition Analysis\textsuperscript{22}

While the risk analysis described above focuses on a single process, not considering where the charging possibly comes from, Process Capability and Transition Analysis (PCTA) looks at the process in total and analyses whether there is charging, that theoretically could result in a discharge during process deviations. Additionally it looks at HBM and MM related problems as well as transitions between process steps. A detailed description can be found in\textsuperscript{23}. This includes the following:

1. Defining the process critical path, identifying key process elements, and their transition points
2. Making transition point measurements
3. Summarizing findings

8.2 Final Test

Final assembled 2.5D and 3D structures of proper design, as addressed earlier in this document, require no extraordinary ESD handing during final test. The common unique element, TSV, are themselves more robust than almost any other connection within the dies. It is important that the guidelines set forth in section 5.3 are followed and applied to the testing environment. Isolated, transiting power rails are a concern and are a potential vulnerability if crisscross rail clamping is not observed. Typically, a completely isolated power rail can be made to withstand $\sim$100V, but there are numerous factors in the design and in the specific process that can affect this. The implementer must take these into account.

Full functional tests are performed for packaged 3D-IC, both during exit control and also after final ESD tests of the packaged IC. The functional testing itself can be a source of a discharge event. Die-die I/O nodes are not stressed directly in this case.

Nevertheless, there are three aspects to be considered regarding die-die I/O of a 3D-IC. Part of the ESD stress at external I/O can be diverted to internal nodes, which is widely reported for single die package designs (non-3D). In the case of 3D-IC these critical internal nodes might often coincide with die-die I/O, if they represent voltage supply domain crossings. However, initial investigations have shown that very basic, inherent protection of the die-die I/O prevents damage due to stress at external I/O\textsuperscript{24}. 
Another challenge of final testing is associated with the analysis capability of a functional test after performing ESD stress qualification. The process of qualification testing requires a full functional test of the DUT prior to stress testing and the final assessment of the functionality of the IC after the stress test. Only if the component passes within the specified data sheet limits can the stress test be rated as valid and passed.

Leakage testing of external I/O in tri-state is a sensitive detector of damage. This cannot be applied to die-die I/O. Only signatures of malfunction or an increase in quiescent supply current can be indicators of damage at die-die I/O. Specific design-for-test measures for 3D-IC need to be developed to improve the analysis capability at die-die I/O.

### 8.3 Qualification

3D/2.5D ESD protection is required for I/O interfaces that provide communication only between die inside a 3D/2.5D package. These 3D/2.5D interfaces are not connected to package pins and thus are internal nodes during industry standard ESD qualification testing. ESD protection of 3D/2.5D interfaces is designed to protect die-to-die I/O during 3D/2.5D assembly.

There is no satisfying data base on required ESD robustness levels for die-die I/O of a 3D-IC available yet. A target level should on one hand comply with the actual stress conditions, but on the other avoid over-engineering because of excessive consumption of silicon area by the on-chip protection. To clarify this, more tests and assessment of the manufacturing steps are required across the industry.

To get to a first recommendation for target ESD levels, the following aspects can be taken into consideration.

State-of-the-art ESD control in manufacturing allows handling parts with minimum 100V HBM robustness (see also S20.20). This provides a good guidance for the required HBM level of die-die I/O.

As CDM type discharge events pose the biggest risk during manufacturing a CDM target level needs to be envisioned as well. The real world CDM stress events occur while the die or the wafer is handled. No specific package type is involved in this stage of manufacturing. For packaged devices a CDM qualification level is defined in terms of voltage. This cannot be applied to bare dies. Instead it is recommended to specify a qualification target in terms of the peak current. Target peak currents between 200mA and 1A are considered to be efficient and practical. Future studies are needed to redefine the target level and to get to a finally aligned target level. This range comes from our best engineering judgment at this point in development, and is for information purposes only.

One way to perform a CDM type qualification test is to mount the die under test in a test package where all internal nodes are routed to package pins. By choosing an appropriate CDM voltage of the simulator the peak current can be adjusted to the required range at the tested internal pins.
However, for designs with a very high number of internal nodes (several thousand) a complete coverage of all pins during an ESD test will be very time consuming, expensive and lead to an unrealistic multi-zap stress. Here a statistical testing of the die-die I/O of same circuit topology is sufficient.

Standard ESD strength of die-to-die I/O is 100V HBM and 20V-30V CDM. Commonly 3D/2.5D ESD protection is designed \textit{a priori} by scaling ESD elements from ESD qualified package I/O interfaces. Each company has its own proprietary approach for both designing HBM and CDM solutions and for scaling.

From the customer’s perspective it is important to know that die-to-die I/O will withstand 100V HBM and 20V-30V CDM. However ESD qualification of die-to-die I/O is not straightforward. These I/O do not have direct access to package pins and therefore established ESD qualification routine is not applicable. A practical qualification solution could be to design an ESD qualification vehicle, where die-to-die I/O are routed to bonding pads and packaged. An ESD vehicle readily allows one to measure the HBM strength of 3D/2.5D ESD protection. This may or may not be practical, depending on architecture complexity.

CDM qualification may produce ambiguous results, as CDM passing voltage is a strong function of both package and die parameters\(^{25}\). Therefore it is recommended to report both CDM passing voltage and corresponding peak current as passing qualification results for die-to-die I/O of a 3D/2.5D device.

Discharges in the manufacturing environment must be controlled by ESD factory control measures which are well implemented in existing semiconductor lines. The safe manufacturing of IC within the limits of well-implemented ESD control is tested by ESD test standards HBM and CDM.

9 Failure Analysis

Assume that we have developed a functional ESD protected 3D-IC system, and that after ESD testing, a failure is observed on one or several I/O pads. What are the Failure Analysis (FA) techniques available to debug the 3D-IC design?

The stacking, interconnecting, and packaging of thinned chips bring several new FA challenges. When before one knew that the failure was somewhere on the chip or in its connection to the package, now one first has to find out whether a failure is on chip level (and which one from the stack), or in the interconnection between the chips, or in the connection to the package. Pinpointing the failure location on chip level becomes much more complicated because of the possible presence of other chips above or below. 3D technology needs the same FA as 2D, but assessing the (different stacked) chips becomes more complicated; new features such as microbumps, TSV, thinned stacked chips, interposers etc. add risks and failure mechanisms, and CPI (chip package interaction),
mechanical, and thermal issues become more important. In Appendix A some possible FA solutions related to 3D technology are discussed.

10 Case Study from Xilinx

Xilinx has been a leader in 2.5D / 3D packaging. In the embedded case study, accepted for the 2015 International ESD Workshop, Xilinx provides insight into a fully functional 2.5D system with ESD protection.

11 Summary & Conclusions

This paper is a result of worldwide collaboration between Global Semiconductor Alliance and ESD Association members, academia, and other industry leaders. This work represents our understanding to date, recognizing that the industry is early in implementing 2.5D / 3D packaging solutions and that no standard ESD test methods exist for HBM or CDM in this packaging environment. As this area matures and our knowledge grows, we expect standards to emerge and EDA tools to incorporate support.

ESD design, protection, test, and analysis is well understood for single die packaging. Standards exist and precautions are followed in the wafer fab and assembly / test facilities. These new packaging paradigms will spawn multiple fab / assembly / test flows. In some cases, portions of the flow will be new to the entity completing the task. This will require increased coordination amongst all parties.

As discussed, there are changes to be considered: ESD susceptibility can be stack architecture dependent; CDM current will flow through all die in the stack; bare die robustness cannot be guaranteed; ESD protection for die-die I/O can be reduced; internal pins for packaged parts cannot be tested for HBM or CDM; HBM current paths are only from external to external pin; TSV will provide inherent protection. These changes do not preclude a safe ESD environment, but do help us understand the precautions required.

As the industry moves to 2.5D / 3D packaging, we recommend following S20.20 / JEDEC standards, and working with EDA vendors to incorporate support in next generation tools. Good collaboration amongst all will be required, as will strong, insightful, system architecture analysis. GSA and ESDA stand ready to help others better understand this environment and build successful devices.
Acknowledgements

GSA wishes to acknowledge the contributions of the following people for their significant contribution and effort to develop and review this paper. Requests for clarifications, corrections, or update should be sent to Harrison Beasley at GSA.

<table>
<thead>
<tr>
<th>Dimitri Linten; imec</th>
<th>Stephen Fairbanks; Certus Semi</th>
</tr>
</thead>
<tbody>
<tr>
<td>Charvaka Duvvury</td>
<td>John Plasterer; PMC-Sierra</td>
</tr>
<tr>
<td>Michael Khazhinsky; Silicon Labs</td>
<td>Roman Gafiteanu; Mentor Graphics</td>
</tr>
<tr>
<td>Andy Lo; Altera</td>
<td>Ting Ku; NVidia</td>
</tr>
<tr>
<td>John Kinnear; IBM</td>
<td>James Karp; Xilinx</td>
</tr>
<tr>
<td>Harald Gossner; Intel</td>
<td>Bart Keppens; Sofics</td>
</tr>
<tr>
<td>Eelco Bergman; ASE</td>
<td>Ramakanth Alapati, GlobalFoundries</td>
</tr>
<tr>
<td>Brandon Wang; Cadence</td>
<td>Reinhold Gaertner, Infineon</td>
</tr>
<tr>
<td>Elyse Rosembaum; University Illinois</td>
<td>Robert Patti, Tezzaron</td>
</tr>
<tr>
<td>Matt Hogan; Mentor Graphics</td>
<td>Gretchen Patti, Tezzaron</td>
</tr>
<tr>
<td>Mujahid Muhammad; IBM</td>
<td>Frank Barber, eSilicon</td>
</tr>
<tr>
<td>Norman Chang; Ansys</td>
<td>Danesh Tavana, Synaptics</td>
</tr>
<tr>
<td>Adam Beece, GlobalFoundries</td>
<td>Harrison Beasley, GSA</td>
</tr>
</tbody>
</table>
13 Appendix A: Possible Failure Analysis Techniques

We discuss six techniques that offer interesting and in some cases very promising applications for failure analysis of 3D stacked IC. End Note 26 applies to every section below, as the paper that demonstrated the claims made in this section.

13.1 X-ray

X-ray imaging remains a very useful technique to study in a non-destructive way microelectronic packages including 3D stacked chips. It was demonstrated\(^\text{26}\) that misalignment between chips, which might cause opens or shorts, can easily be detected. Also micron-sized voids in TSV can be detected. A problem remains in that the spatial resolution of the technique is limited. X-ray microscopy combined with tomography offers a better resolution, but only for small sample sizes. In addition it is very time consuming.

13.2 Scanning acoustic microscopy

Scanning acoustic microscopy (SAM) is very useful to detect delamination or voids. As for X-ray, conventional SAM has limited spatial resolution. This can be increased by using higher frequency transducers. When imaging with GHz frequencies, SAM offers some new possibilities for 3D failure analysis. It can detect voids in a TSV (see for example Figure 1), and offers information on microbump failures.

![GHz SAM image showing the presence of voids in TSV.](image)

13.3 IR laser scanning microscopy

If the Si chip surface is not rough, IR microscopy can be used to look through a chip to check for example alignment problems (see Figure 2). IR has also the drawback however that the light cannot penetrate through metals or some underfill materials. It can be used to pinpoint the exact location of a suspected failure site for FIB opening, which we applied to study a defective Kelvin structure (see Figure 3).
Magnetic field imaging

One of the most promising techniques for 3D FA is magnetic field imaging (MFI)\textsuperscript{27}. This technique measures the magnetic field associated with an electrical current using a scanning sensor. The magnetic image then allows one to visualize the current path. The technique can measure through the package but also through stacked chips. Figure 4a shows the location of a short in a daisy chain between two stacked IC, measured through the backside of a full thickness top chip. Figure 4b shows how the technique was used to pinpoint a short related to a design error. Not only shorts but also opens can be detected using space domain reflectometry. Examples obtained on packages off stacked chips will be discussed in the paper.
13.5 Photon emission microscopy

Photon emission microscopy (PEM) detects light emitted by biased devices. Possible emission sources are field accelerated carriers, radiant electron-hole recombination and blackbody radiation. The main problem with PEM is that metal layers can prevent the observation of emission. For 2D technology, a solution is backside PEM. For 3D technology this is not straightforward. If only two chips are present, depending on the stacking (face to face or back to face) it might be possible that PEM can still be used. However, for 3D in general it will require delayering of the stack while still ensuring electrical access. This is complicated because of the fragile thinned chips and the presence of bumps and underfill material between each two chips of the stack. PEM can be done from the side\textsuperscript{28} if the failure is for example located in the liner of a TSV close to the edge of a chip. In the paper we will demonstrate that, when using FIB for sample preparation, PEM might indeed be applicable for some failure detection in 3D stacks. Fig. 5 shows a PEM image of a failure site located near the bottom of a TSV.

![](image.png)

**Figure 5 PEM study of liner breakdown in a TSV**

13.6 Lock-in thermography

A promising technique for 3D FA, even for packaged chips, is lock-in thermography. This technique can detect shorts and opens. It needs a correct activation of thermally active defects. It was shown to be able to detect hot spots through overmould material.
References

1 Electrostatic Discharge (ESD) Technology Roadmap – Revised March 2013
2 Makoto Nagata, et al.; “CDM Protection of a 3D TSV Memory IC with a 100 GB/s Wide I/O Data Bus”
5 Makoto Nagata, et al.; “CDM Protection of a 3D TSV Memory IC with a 100 GB/s Wide I/O Data Bus”
6 E. Rosenbaum, UIUC / Workshop on ESD Challenges for 3D IC
10 Frank Feng, “My Design’s Interconnect Has Enough Wire Width to Withstand ESD... Doesn’t It?”, SemiMD, October 2014
14 Matthew Hogan, Dusan Petranovic “Robust Verification of 3D-ICs: Pros, Cons and Recommendations”, in Proceedings of IEEE 3DIC Conference, 2009
15 Matthew Hogan, Dusan Petranovic “Robust Verification of 3D-ICs: Pros, Cons and Recommendations”, in Proceedings of IEEE 3DIC Conference, 2009
17 E. Rosenbaum, UIUC / Workshop on ESD Challenges for 3D IC
18 Andrew Olney, et al.; “Real-World Charged Board Model (CBM) Failures”
21 [A] R. Gaertner, Do we expect ESD-failures in an EPA designed according to international standards? The need for a process related risk analysis; EOS/ESD Symposium 2007


24 Scholz et al EOSED 2014 "CDM protection of a 3D TSV memory IC with a 100 GB/s wide I/O data bus"


26 Ingrid De Wolf, et al “Failure Analysis Challenges for 3D Stacked ICs”, 8th Annual International Electrostatic Discharge Workshop
