Effective Post-TSV-DRIE Wet Clean Process for Through Silicon Via Applications

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Veeco Clean Process Sequence in WaferStorm®

Veeco Wet Clean Process:
• Immersion batch soak in Dynastrip™ DL9150
• Single wafer high pressure fan spray with Dynastrip™ DL9150
• Rinse and spin dry

Electrical test was used to evaluate the performance of the cleaning process. Arrays of TSVs are connected to bond pads on the front surface of the wafer. Voltage is applied and leakage current is measured to the substrate. Voltage is then ramped in step pattern to determine voltage where TSV dielectric breakdown occurs.

Fluorine peak is not present after the clean

Results discussion
Auger Electron Spectroscopy was used to examine the 2x40 µm TSV sidewalls before and after cleaning. Data are shown for the 1800 second soak/SC1 rinse process split. Three locations inside the TSV were measured (top, middle, bottom). Background levels were obtained from freshly cleaved silicon next to the TSV (“off TSV”). Electrical test was done on 32 dies per wafer. Veeco wet clean had average leakage current approximately the same as POR. The split cell “no clean” wafers (without a wet clean) performed similarly to POR for the wafers with the Ash process. Without the Ash process the results are quite different indicating the sidewall polymer is removed primarily by the Ash in the POR. For the Veeco wet clean there is no difference without Ash.

Conclusions
• Electrical and physical analysis shows the Veeco wet clean removes both the photoresist and sidewall polymer residues from the TSVs.
• The new clean process can replace the ash, reducing the TSV RIE process time by 33%.

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